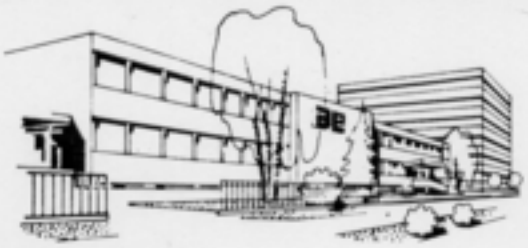
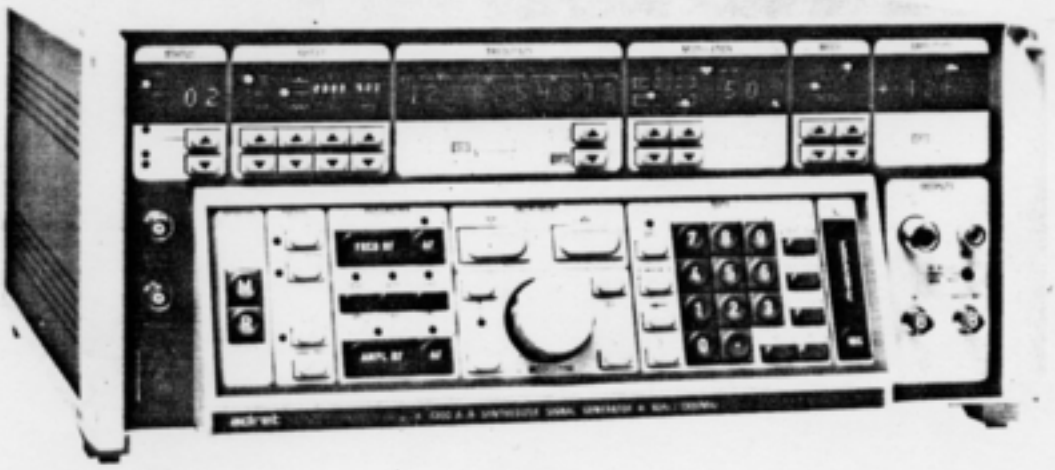
adret electronique®





VHF/UHF GENERATOR
10Hz/1300 MHz

with AM, FM and ΦM modulation facilities

7200A

adret electronique®
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INDEX

CHAPTER VI : MAINTENANCE

CHAPTER V

MAINTENANCE

GENERAL

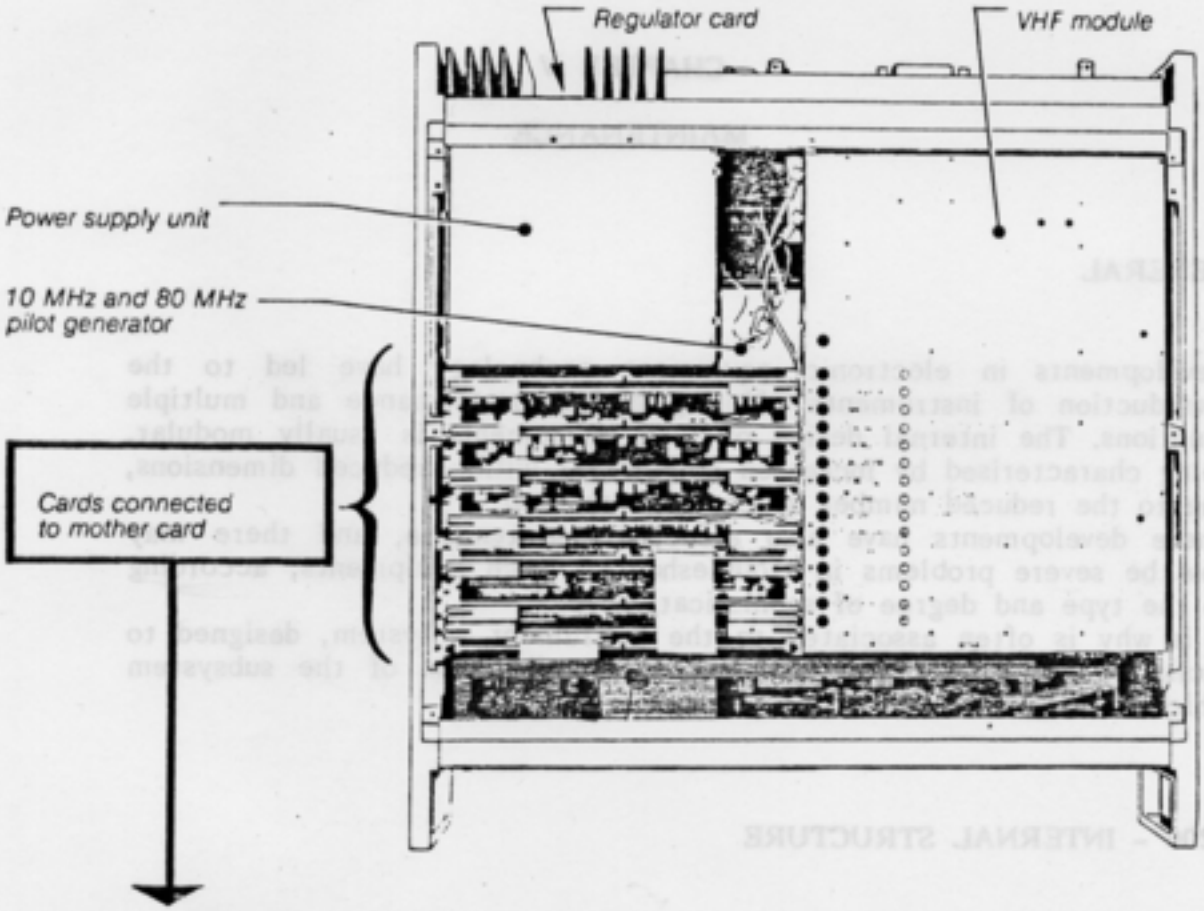
Developments in electronic equipment technology have led to the introduction of instruments offering higher performance and multiple functions. The internal design of such instruments is usually modular, being characterised by increased complexity within reduced dimensions, due to the reduced number of components used.
These developments have also affected maintenance, and there may now be severe problems in troubleshooting such equipments, according to the type and degree of sophistication.
It is why is often associated to the instrument a system, designed to facilitate maintenance by providing a fast diagnosis of the subsystem which has failed.

7200 - INTERNAL STRUCTURE

The ADRET 7200 VHF/UHF signal generator is a modular instrument comprising boards which plug into a mother board and plug-in modules in light alloy enclosures. This form of packaging is particulary used for HF circuits to maintain spectral purity specifications in spite of the high operating levels.
Modular internal structure offers a number of advantages some of which are relevant to maintenance :
- the sub-assembly swapping facility avoiding instrument down time,
- the circuit accessibility for the servicing,
- the faster check of running signals by the control points grouping.

Maintenance is further simplified by the inclusion of a self-test system controlled by the inbuilt microprocessor.
This system, enabled while troubled shooting, gives for each point tested whether the signal is correct or not.
The self-test results are not sufficient to produce a definite diagnosis of a subsystem malfunction, but are needed to enable that part of the instrument which has failed to be identified and located.

MODULAR DESIGN...



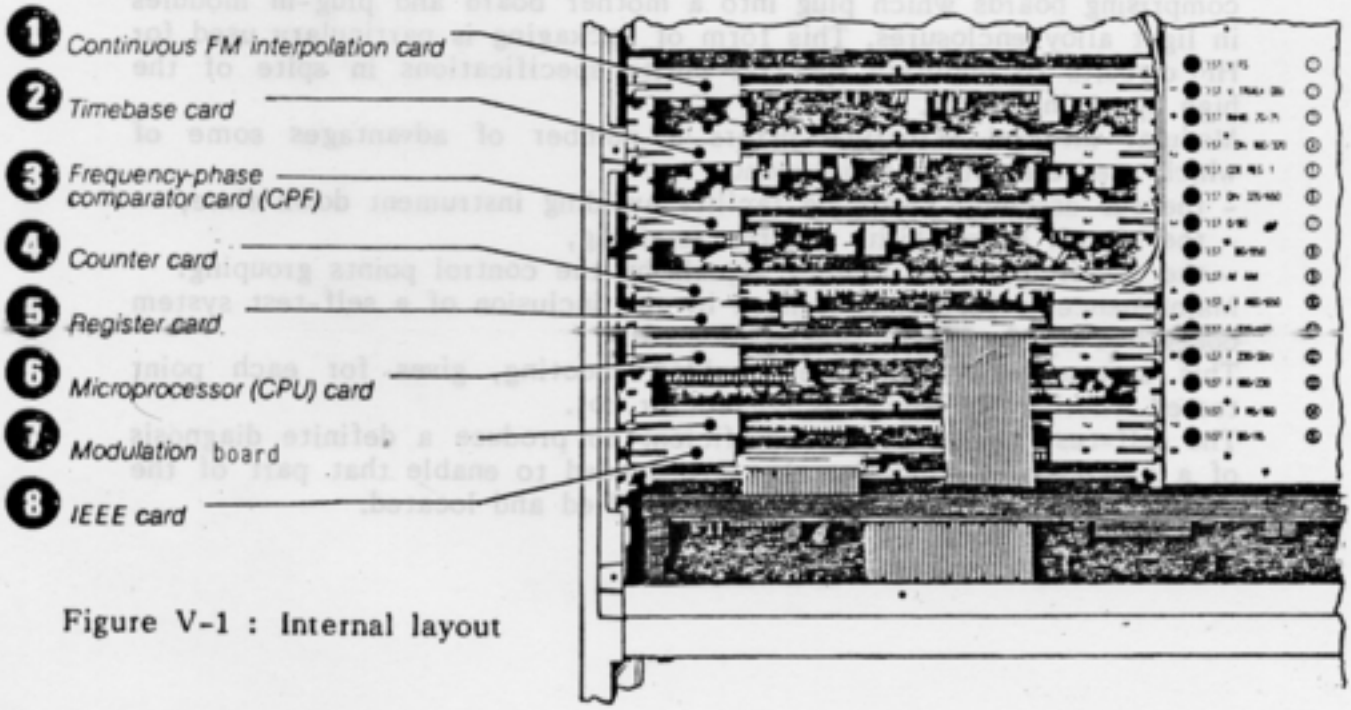


Figure V-1 : Internal layout

...FOR ENHANCED INTERCHANGEABILITY

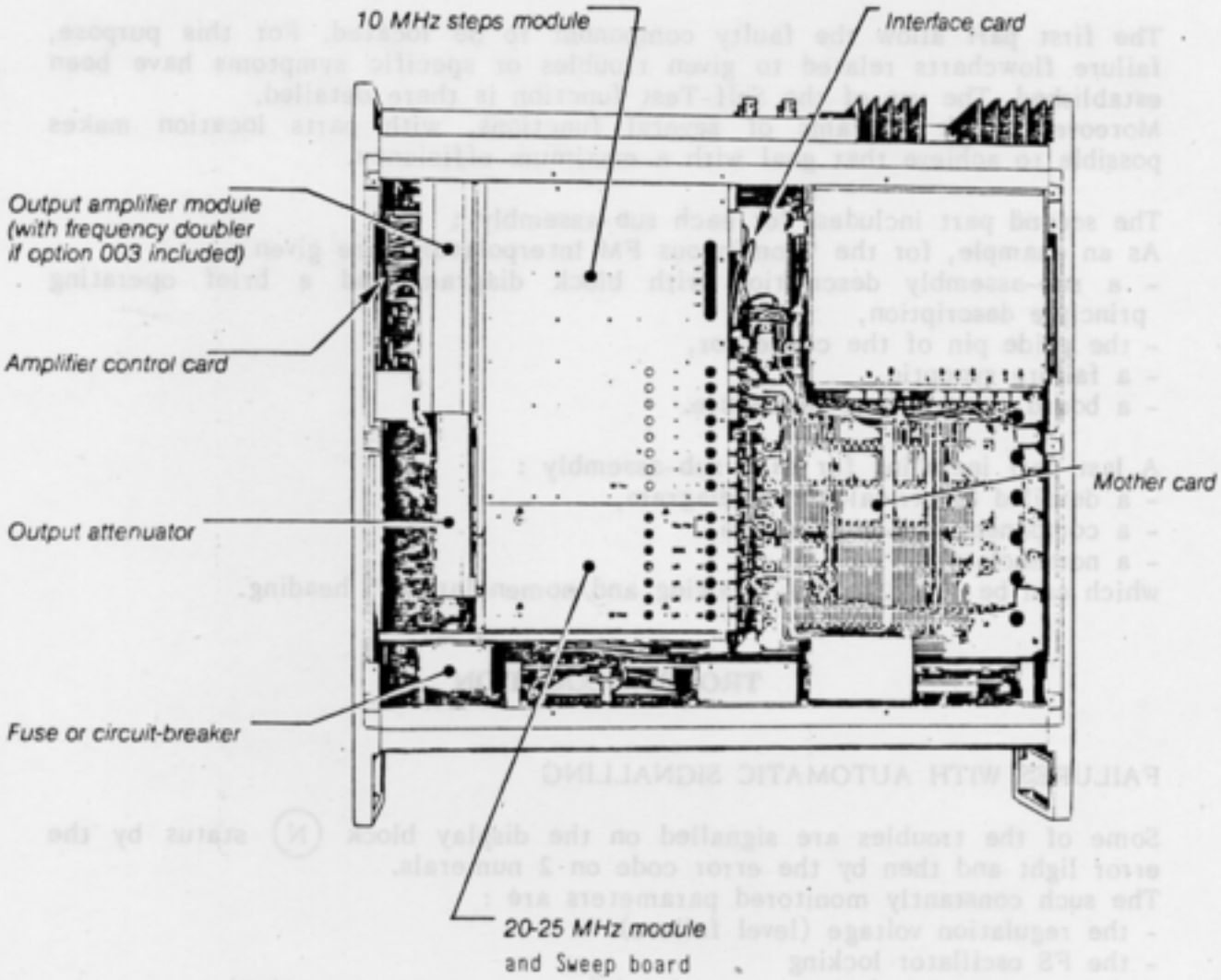


Figure V-2 : Internal layout

TROUBLESHOOTING PROCEDURE

The "**MAINTENANCE**" chapter is broken down into two distinct parts, corresponding to a logical process in the servicing operations.

The first part allow the faulty component to be located. For this purpose, failure flowcharts related to given troubles or specific symptoms have been established. The use of the Self-Test function is there detailed.
Moreover, block diagrams of several functions, with parts location makes possible to achieve that goal with a maximum efficiency.

The second part includes, for each sub-assembly :
As an example, for the "Continuous FM Interpolator", are given :
- a sub-assembly description with block diagram and a brief operating principle description,
- the guide pin of the connector,
- a failure synoptic,
- a board check-adjust procedure.

A last part including for each sub-assembly :
- a detailed electrical wiring diagram,
- a component lay-out diagram,
- a nomenclature,

which can be found in the "drawing and nomenclatures" heading.

TROUBLE LOCATION

FAILURES WITH AUTOMATIC SIGNALLING

Some of the troubles are signalled on the display block (N) status by the error light and then by the error code on 2 numerals.
The such constantly monitored parameters are :
- the regulation voltage (level failure)
- the FS oscillator locking
- the permanence of the output signal (reverse power protection).

In programming mode, a trouble on one of the above parameters, is signalled in sending a SRQ on the bus.

SELF - TEST

Enabling the self-test facility verifies the internal operation of the generator by checking the level at 11 test points (see table below), the locations of which are specified on the detailed block schematic of the instrument.

Associated with these 12 test points are six indicator lamps which show that the signal monitored in test 08 is not locked on, which signal is faulty (FP or FS) and the microprocessor operational status (test 10). The positions of these indicator lamps are shown on Figure V-3.

Test No	Function	Card or module
00	2 MHz or 2 MHz ± ε from VERNIER	Phase-frequency comparators
01	FP/40 output (FP designates 300 - 670 MHz oscillator output frequency	10 MHz steps
02	300 - 670 MHz output	10 MHz steps
03	VHF module regulation voltage 1	Interface
04	20 - 25 MHz output	Interconnection card
05	Output FS/40 (FS designates 320 - 650 MHz oscillator output frequency)	VHF module
06	400 MHz output	10 MHz steps
07	20/25 MHz sum/difference frequency	VHF module
08	Locking of 20 - 25 MHz oscillator to 1 kHz	Counters card
09	4 MHz sum/difference frequency	Phase-frequency comparators
10	FS and FP, lock-on	Frequency-phase comparators
11	Circuit-breaker open (from series B7)	Circuit-breaker option 002

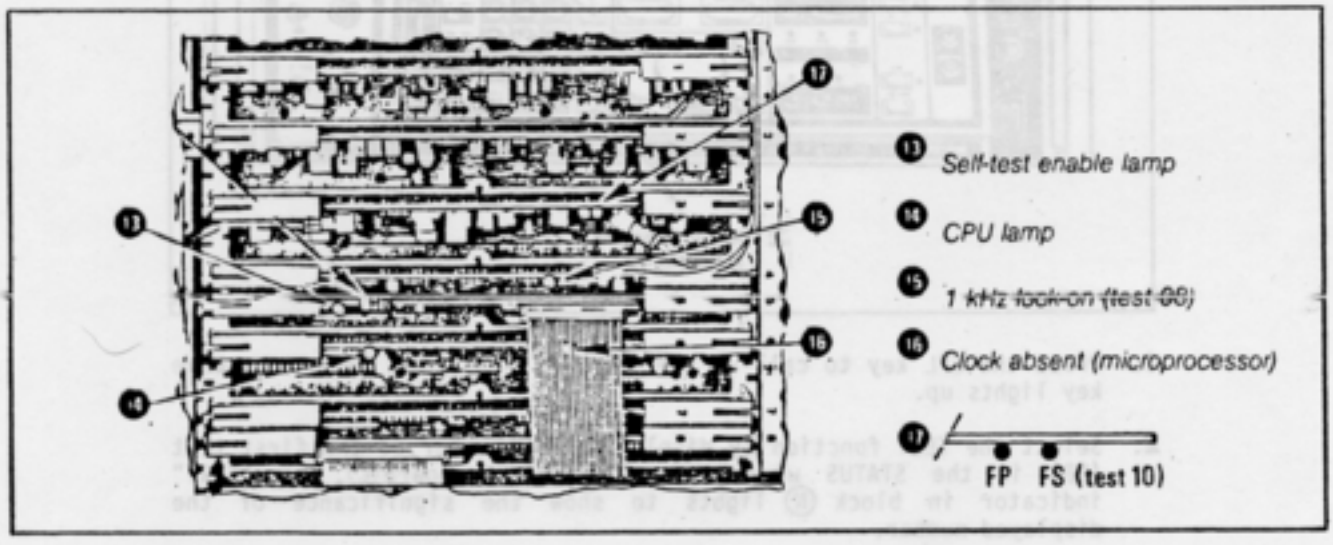


Figure V-3 : Layout of test indicator lamps

• The CPU indicator lamp flashes whenever the microprocessor is activated, the scanning phase being triggered by any operation of the front panel controls.
• The "clock absent" lamp comes on if the clock signal from the controlling unit is incorrect.
• The "1 kHz lock-on" lamp comes on when the result of test 08 is negative
• The "FP-FS" lamps indicate which signal is responsible for the negative result of test 10. Lamp "FS" comes on when it is the output signal of the 320/650 MHz oscillator. Both lamps come on when it is the output signal of the 300/670 MHz oscillator.

SELF-TEST ENABLING

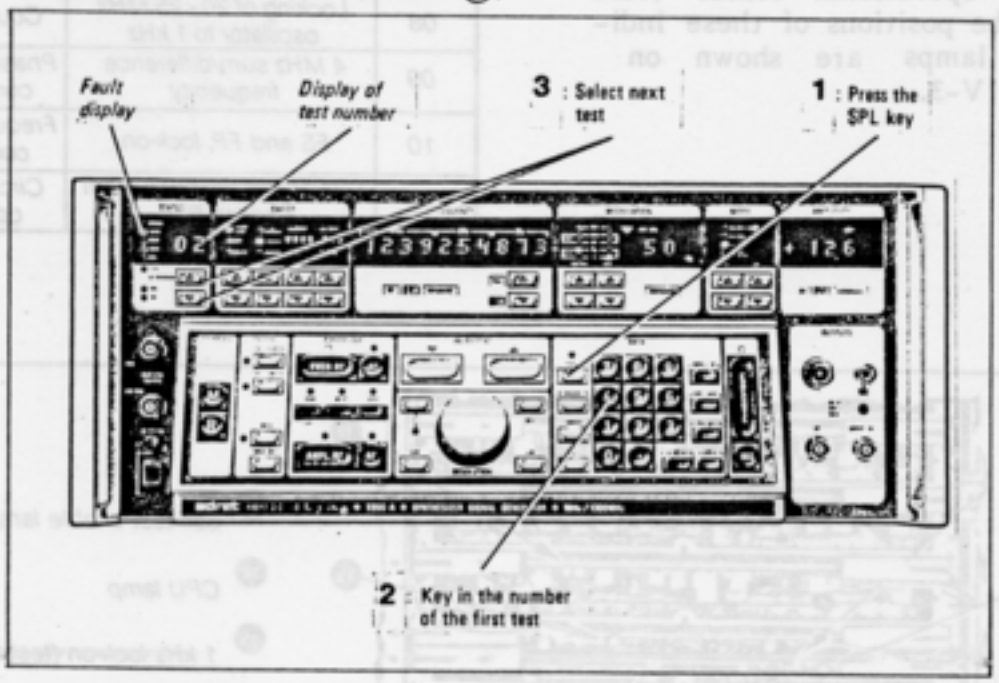
AUTOMATIC TEST

The TEST/SELF TEST function is automatic for tests Ø3, Ø8, 1Ø and 11 in which the generator permanently self-checks. When one of those tests fails, a continuous audible signal is produced (buzzer) and the error code for the defective point appears in the STATUS block display Ⓝ.

The ERROR indicator in block Ⓝ lights to show that the "self-check" has detected a fault during the four-test phase.

MANUAL TEST

Test points that are not checked automatically are monitored manually in LOCAL or REMOTE mode, any fault being signalled by the lighting of the "ERROR" indicator in STATUS block Ⓝ.



1. Press the SPL key to call up special functions. The indicator above key lights up.

2. Select the TEST function by displaying the number of the first test (ØØ) in the STATUS window Ⓝ using the keyboard Ⓒ. The "TEST" indicator in block Ⓝ lights to show the significance of the displayed number.

3. Select the next test and repeat the check. The upper key in block Ⓝ increments the test code from ØØ to 11. The lower key decrements the test code.

INHIBITING THE TEST FUNCTION

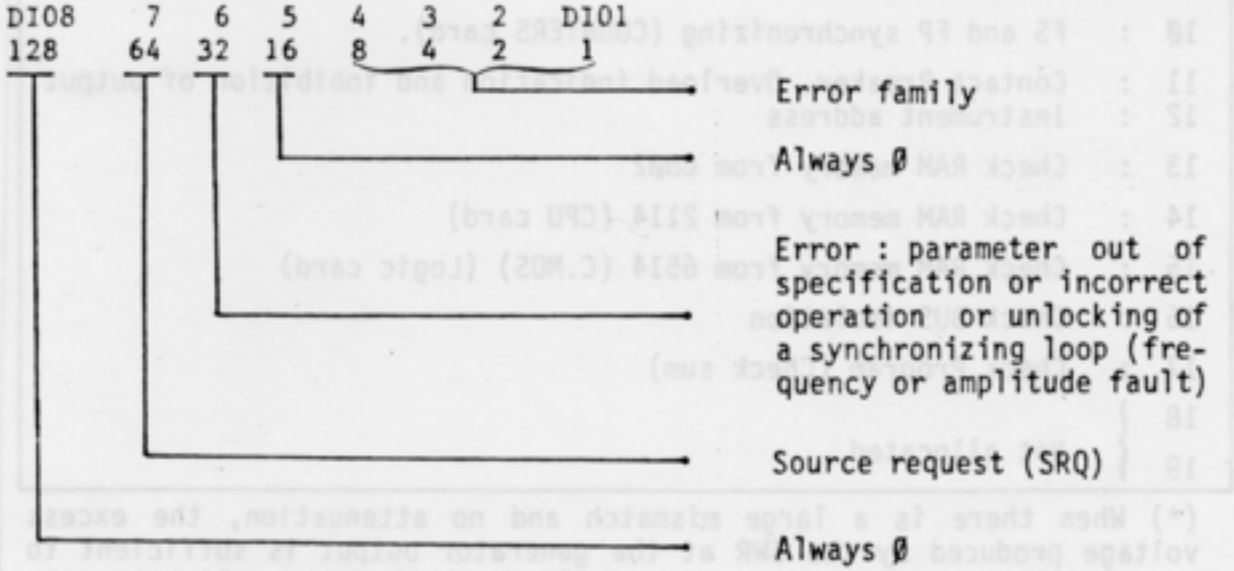
The function is inhibited by pressing the "SPL" and "C" keys on the keyboard Ⓒ.

TEST / SELF-TEST ERROR CODES

STATUS (STATUS READ OUT)

The equipment performs function SR1 of the IEEE-488 standard by transmitting the signal SRQ (source request) on the BUS following any attempt to exceed the input specifications or when a synchronizing loop becomes unbalanced.

The controller can then request a status byte according to the serial polling procedure.
The byte format is as follows :
Setting bit 6 indicates an application fault, or a functional fault that has caused a synchronizing loop to become unlocked. The error code family (0 to 9) is indicated in bits 1-2-3-4.



* On interrupt request (rsv), the complete error code can be obtained in programming the "ER" prefix followed by a BUS reading by the controller.

EXAMPLES :

```
wrt 7ØØ, "F2e9      : RF frequency overtaking
rds (7ØØ)           : status = rsv + error + family 2
wrt 7ØØ, "ER"       : error code request
red 7ØØ, A          : A = complete error code
```

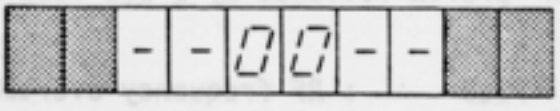
Test / Self-test

The generator is fitted with a TEST device which tests the functioning of the sub-assemblies and facilitates maintenance operations by fault localization.
The device checks the main internal signals which are listed below and given two-figure numerical codes.

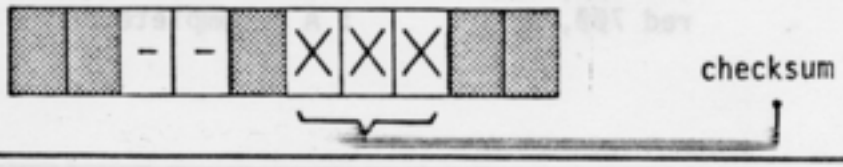
ØØ	:	2 MHz reference input level or level of the 2 MHz ± ΔF output from the vernier.
Ø1	:	FP/40 output level from the "10 MHz STEP" module.
Ø2	:	"10 MHz STEP" module output level.
Ø3	:	VHF module output level.
Ø4	:	"20 to 25 MHz OSCILLATOR" module output level.
Ø5	:	FS/40 output level from the "VHF" module.
Ø6	:	400 MHz output level ("10 MHz STEP" module) This signal is only validated when the output frequency is lower than 80 MHz.
Ø7	:	Level of the 20/25 MHz beat frequency (VHF module) between the 300/670 and 320/650 MHz oscillators.
Ø8	:	Synchronizing the 20/25 MHz oscillator at 1 kHz.
Ø9	:	Level of 4 MHz beat frequency ("PHASE-FREQUENCY COMPARATOR" card)
1Ø	:	FS and FP synchronizing (COUNTERS card).
11	:	Contact Breaker. Overload indication and inhibition of output *
12	:	Instrument address
13	:	Check RAM memory from 68Ø2
14	:	Check RAM memory from 2114 (CPU card)
15	:	Check RAM memory from 6514 (C.MOS) (Logic card)
16	:	Check BUS isolation
17	:	Check Program (Check sum)
18	}	Not allocated
19	}	

(*) When there is a large mismatch and no attenuation, the excess voltage produced by the SWR at the generator output is sufficient to operate the contact breaker. The fault is indicated by lighting the "ERROR" indicator in block (N).

On a request of address, the block E is displaying :

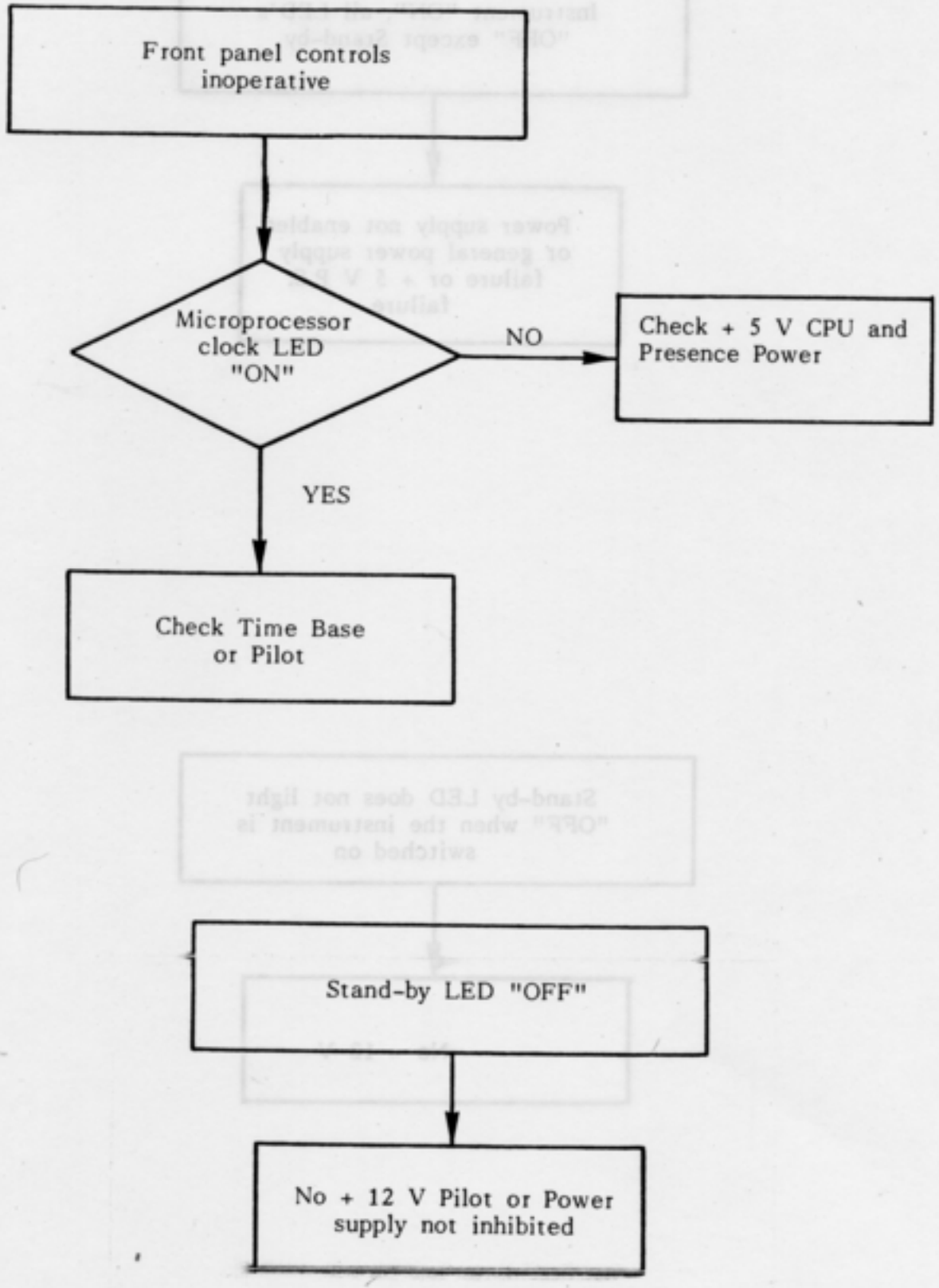


On a request of checksum, the block E is displaying :



TROUBLESHOOTING CHARTS

FRONT PANEL



Instrument "ON", all LED's "OFF" except Stand-by

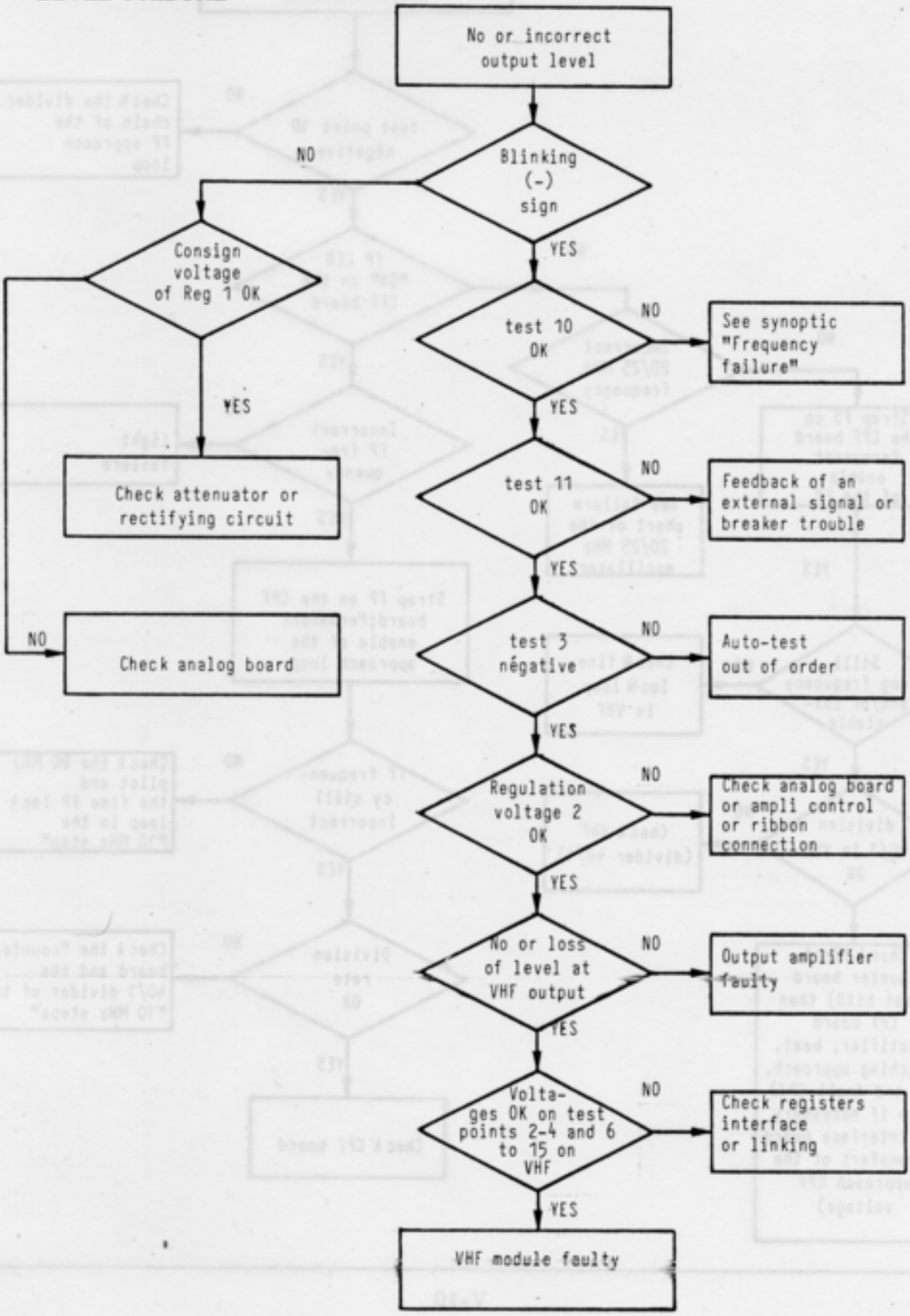
Power supply not enabled or general power supply failure or + 5 V P.S. failure

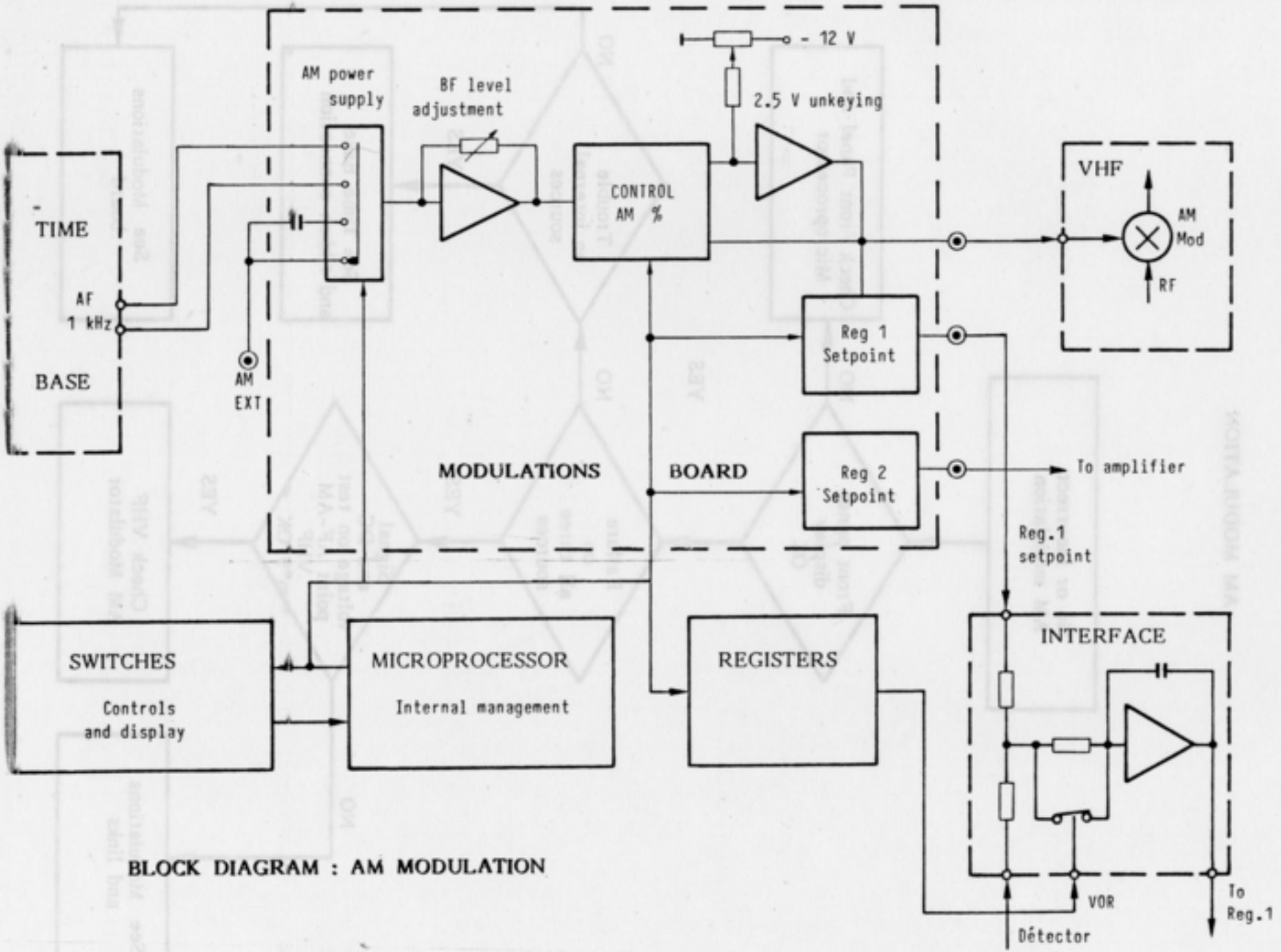
Stand-by LED does not light "OFF" when the instrument is switched on

No - 12 V

FREQUENCY FAILURE

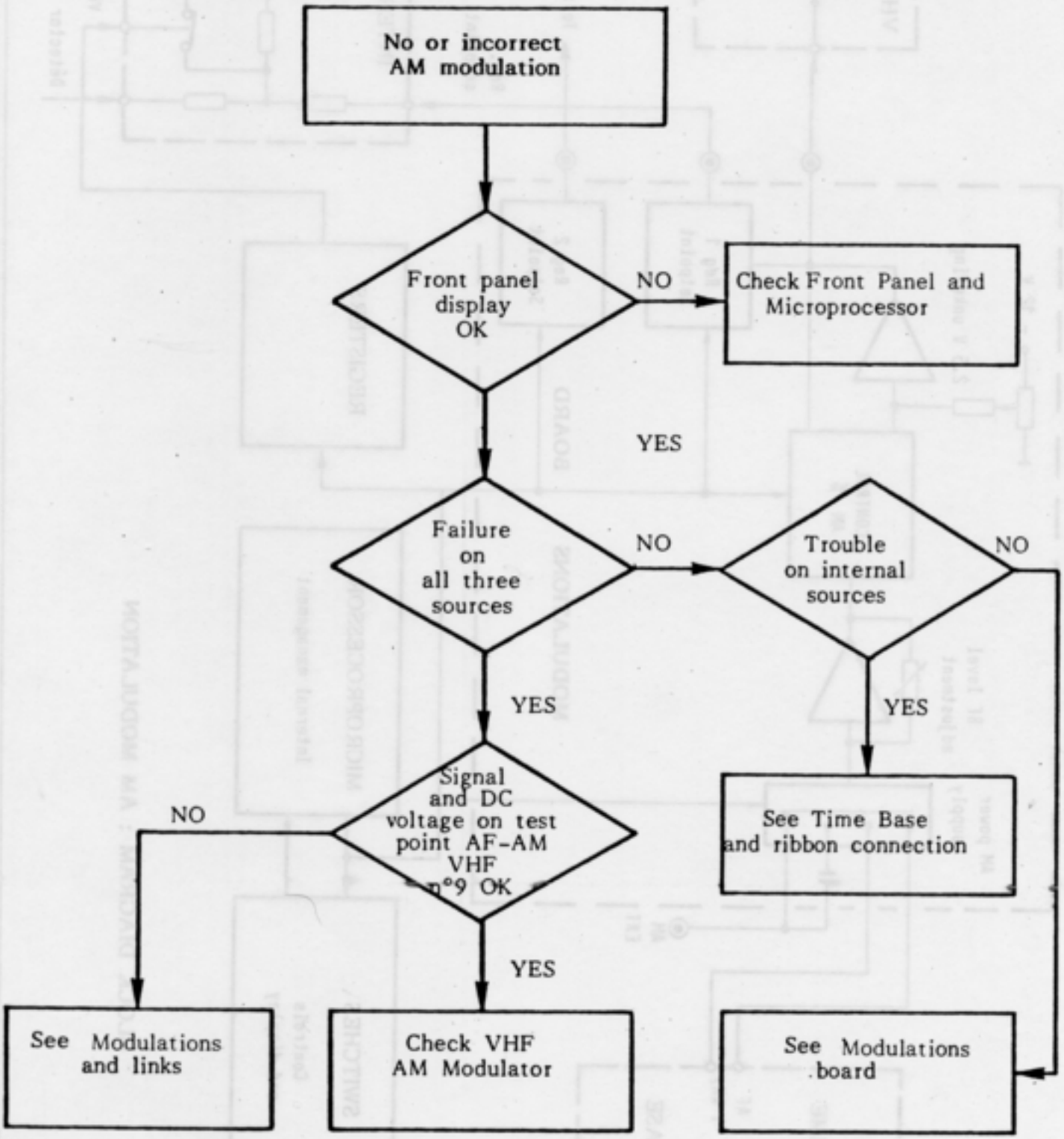
LEVEL FAILURE



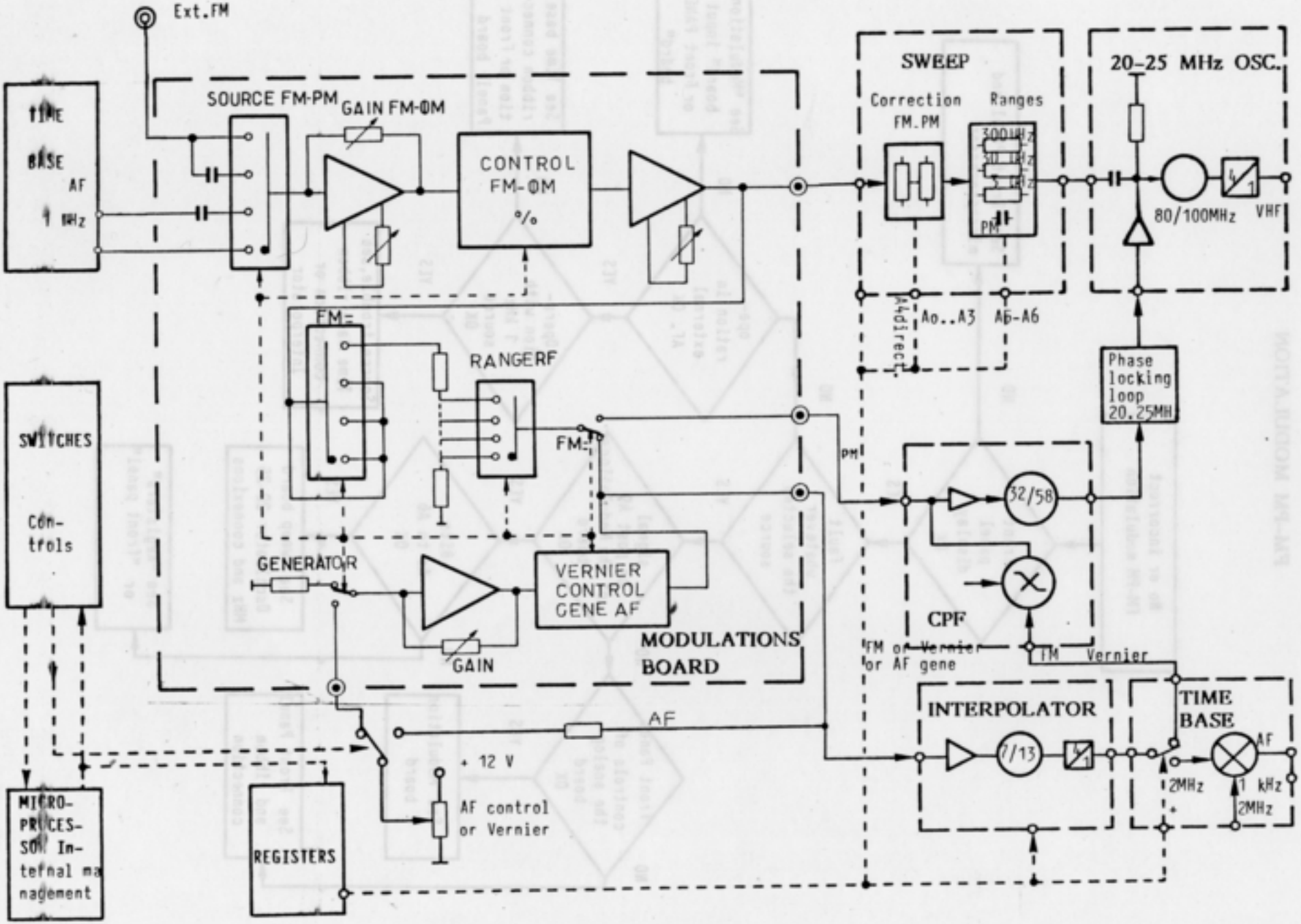


BLOCK DIAGRAM : AM MODULATION

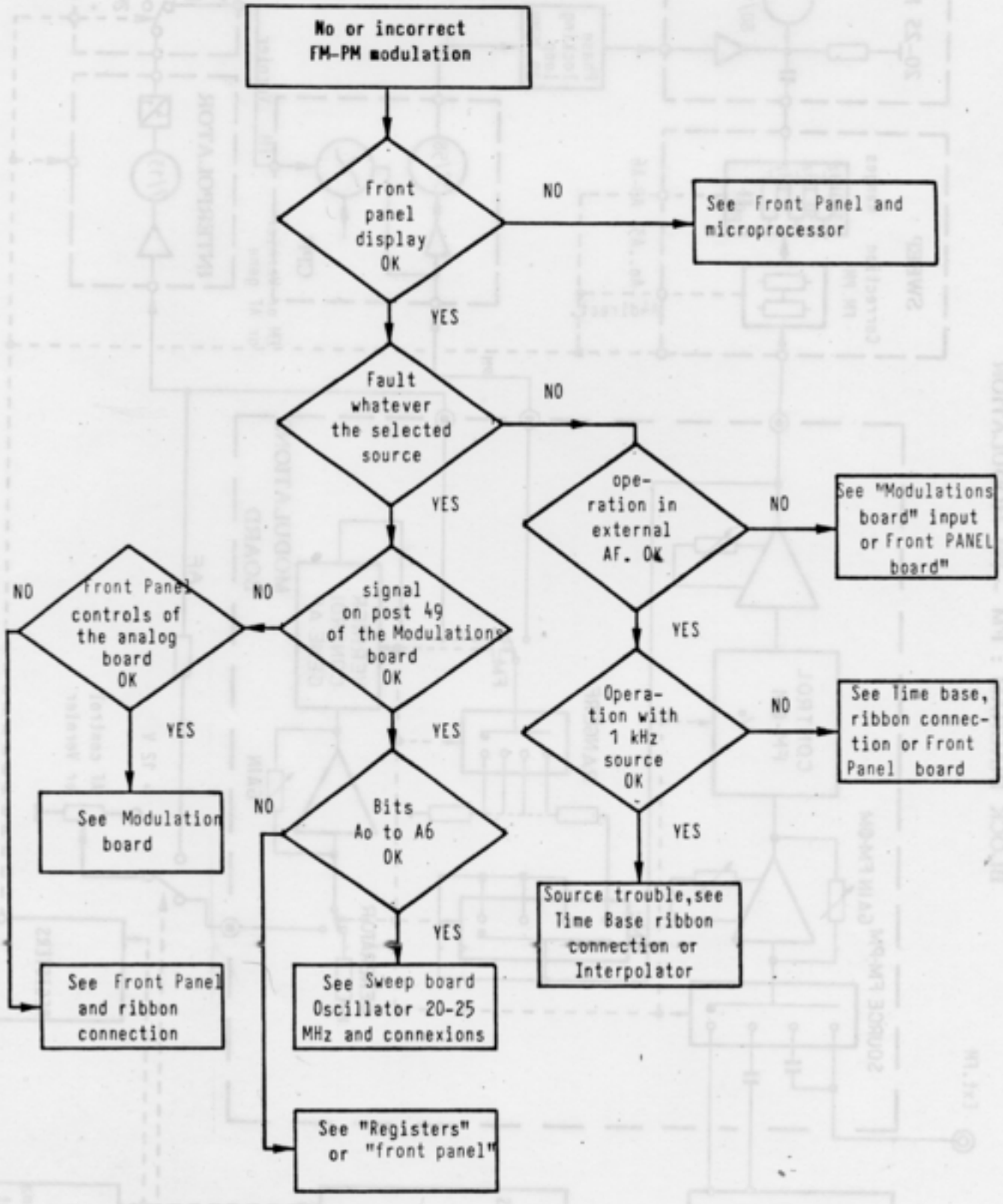
AM MODULATION



BLOCK DIAGRAM : FM - PM MODULATION



FM-PM MODULATION



CONTINUOUS FM INTERPOLATOR

The INTERPOLATOR subsystem provides frequency resolution down to 1 Hz or frequency modulation at frequencies down to 0 Hz (DC). These two functions are obtained by substituting a frequency of 2 MHz ± ΔF for the 2 MHz reference frequency input to the PHASE-FREQUENCY COMPARATOR subsystem.
It provides AF signal generating too, by mixing it output frequency with the 2 MHz of TIME BASE.

The frequency 2 MHz ± ΔF is obtained by dividing by 5 in integrated circuit SN8 a frequency 10 MHz ± 3 obtained from the 7/13 MHz interpolation oscillator. According to the selected DC FM range, the frequency output from this oscillator is input directly to the divide by 5 circuit (300 kHz range), or first modified by one or two increment dividers (30 and 3 kHz ranges and **VERNIER** range). The value of this frequency is also dependent on the frequency synthesised by the generator, as indicated in the table below :

Carrier frequency	Interpolation frequency
< 80 MHz	10 MHz ± 750 kHz
80 MHz/160 MHz	10 MHz ± 3 MHz
160 MHz/320 MHz	10 MHz ± 1.5 MHz
320 MHz/650 MHz	10 MHz ± 750 kHz
650 MHz/1.3 GHz	10 MHz ± 375 kHz

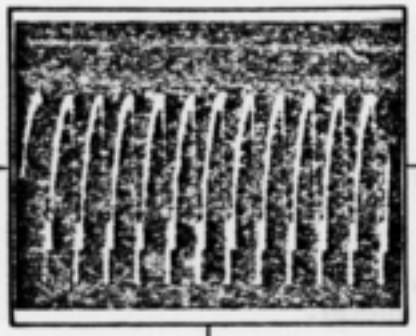
Each increment divider comprises a divide by 10 circuit (SN4 and SN6) followed by an active lowpass filter. A TBA 673 mixer receives the active filter output frequency and a frequency of 9 MHz from the TIME BASE. The sum product is selected by a bandpass filter centred on 10 MHz to provide a signal whose frequency increment relative to 10 MHz is divided by 10.

The frequency generated by the interpolation oscillator is divided by 4 in integrated circuit SN3 then input to the MC 6840 frequency meter of the **CPU** subsystem in order to display the 1 Hz, 10 Hz and 100 Hz steps of the generator output frequency, when the vernier, the DC FM or AF generator frequency is used.
The frequency/voltage converter, downstream situated, is made of an integrated circuit SN9 which stabilizes the oscillator, by comparison with a reference voltage and integration of the result. This convertor makes profit of a characteristic of Cmos gates, the drawn power of which is proportionnal to the transitions number, and therefore to the frequency. The total deviation of the oscillator, i.e. ± 3 MHz. is achieved in feeding a ± 0.5 mA on the pin 1 of the connector.

TROUBLESHOOTING CHART

Use oscilloscope to test

Enable VERNIER and test presence of 10 MHz signal at collector of Q3 (see oscillogram 1)

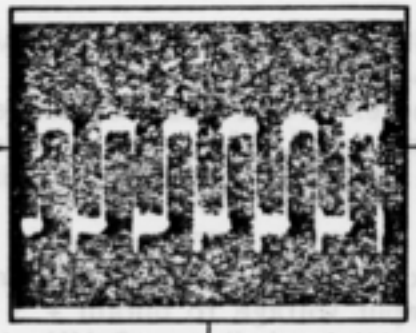


4.5V

NO → See 7/13 MHz oscillator and signal shaping circuits

YES

Signal at 2.5 MHz ± Δf at pin 9 of integrated circuit SN3 (see oscillogram 2)



3.3V

NO → See logic switch and décoder SN1, SN2

YES

9 MHz signal at test points PT06 and PT12 (level ⩾ 340 mVcc)

NO → See separators or Time base board

YES

FM = modulation and 300 kHz range, signal at 2 MHz ± Δf at PT16 (see oscillogram 3)

3.6V

NO → See logic switches and dividers (SN8-SN7-SN5)

YES

Select 30 kHz range on front panel and vérify 2 MHz ± Δf at PT16

NO → See divider SN4, adder mixer, signal-shaping circuit, filter

YES

Select 3 kHz range and test PT16 again

NO → See divider SN6 and adder mixer

ADJUSTMENTS

BOARD REPAIRED

Equipment required :

- oscilloscope,
- DC voltage source,
- 20 MHz frequency meter,
- multimeter.

1. 7 - 13 MHz oscillator

a) Set frequency 100 MHz and disable frequency VERNIER control
b) Select function FM = and 3 kHz range
c) Connect frequency meter to PT1 and DC voltmeter to pin 6 of SN12
d) Apply to FM-ØM input DC voltage to produce 0.000 V reading on voltmeter. Adjust P1 to obtain reading 10 MHz ± 1 kHz on frequency meter
e) Apply DC voltage to obtain - 5 V reading on voltmeter. Adjust P2 to obtain 13 MHz ± 1 kHz reading on frequency meter
f) Reverse polarity of input voltage to obtain + 5 V reading on voltmeter. Verify that frequency meter indicates 7 MHz ± 20 kHz
g) Connect voltmeter to PT2 and adjust T1 to obtain reading of 3 V
h) Repeat (e) to obtain frequency meter reading of 13 MHz and verify that level at PT2 is $\leqslant$ 9.8V. Adjust T1 to obtain a level of 9.8 V
i) Connect oscilloscope to PT1 and verify that the level at 13 MHz is $\leqslant$ 1.4 Vpp
k) Repeat (f) to obtain frequency meter reading of 7 MHz and verify that the level at PT2 is $\geqslant$ 2.2 V

2. Timebase 9 MHz output

a) Connect oscillator probe to PT6 and adjust T4 to obtain maximum level ($\geqslant$ 340 mVpp)
b) Connect probe to PT12 and adjust T5 to obtain maximum level ($\geqslant$ 340 mVpp)

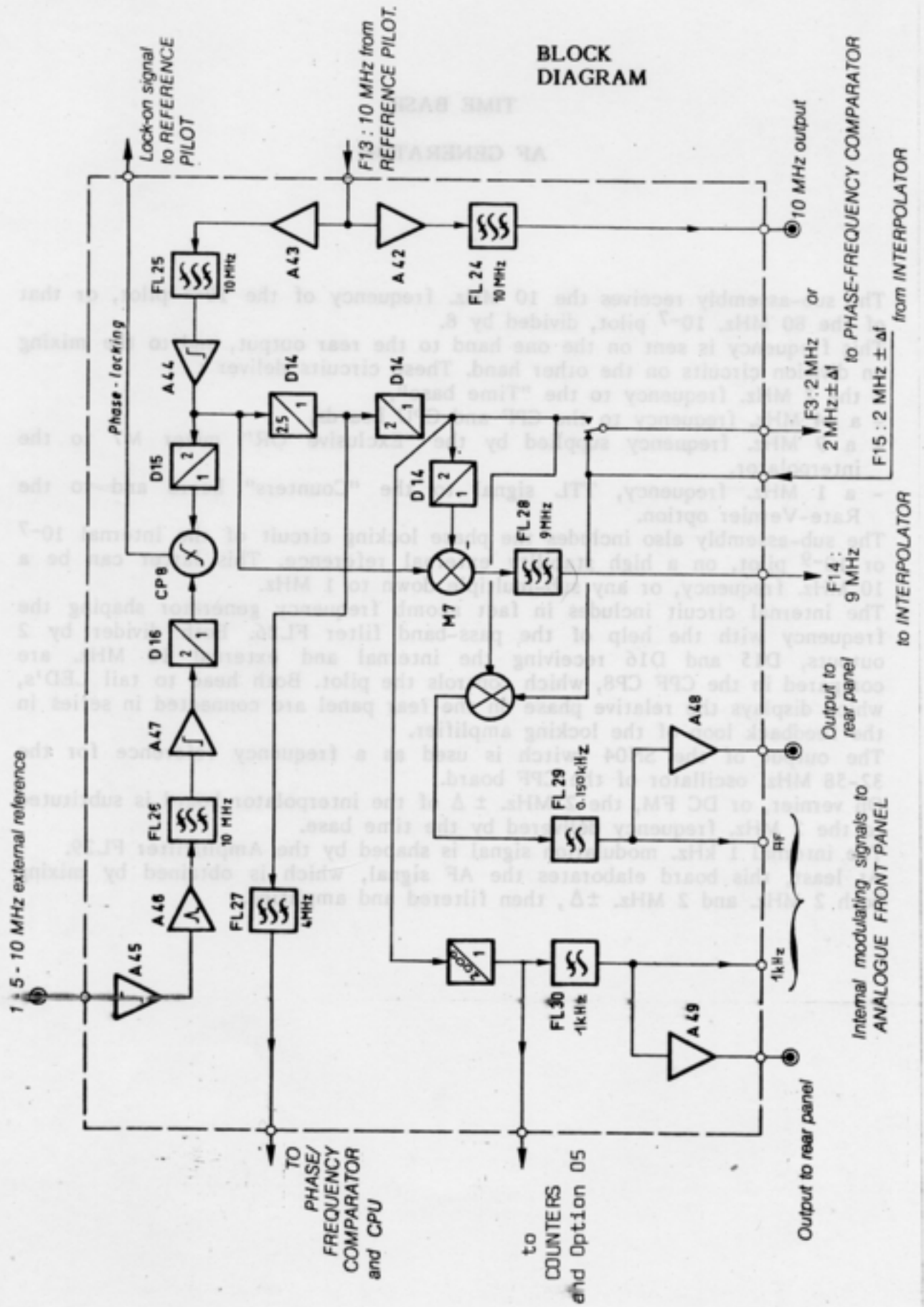
For the calibration, see chapter V, paragraph 9.

TIME BASE

AF GENERATOR

The sub-assembly receives the 10 MHz. frequency of the 10^{-9} pilot, or that of the 80 MHz. 10^{-7} pilot, divided by 8.
This frequency is sent on the one hand to the rear output, and to the mixing an division circuits on the other hand. These circuits deliver :
- the 2 MHz. frequency to the "Time base",
- a 4 MHz. frequency to the CPF and CPU boards,
- a 9 MHz. frequency supplied by the "Exclusive OR" mixer M7 to the interpolator,
- a 1 MHz. frequency, TTL signal to the "Counters" board and to the Rate-Vernier option.

The sub-assembly also includes the phase locking circuit of the internal 10^{-7} or 10^{-9} pilot, on a high stability external reference. This latter can be a 10 MHz. frequency, or any sub-multiple down to 1 MHz.
The internal circuit includes in fact acomb frequency generator shaping the frequency with the help of the pass-band filter FL26. Both divider by 2 outputs, D15 and D16 receiving the internal and external 10 MHz. are compared in the CPF CP8, which controls the pilot. Both head to tail LED's, which displays the relative phase on the rear panel are connected in series in the feedback loop of the locking amplifier.
The output of the SN04 switch is used as a frequency reference for the 32-58 MHz. oscillator of the CPF board.
On vernier, or DC FM, the 2 MHz. $\pm \Delta$ of the interpolator board is subtituted to the 2 MHz. frequency delivered by the time base.
The internal 1 kHz. modulation signal is shaped by the Ampli/filter FL29.
At least, this board elaborates the AF signal, which is obtained by mixing both 2 MHz. and 2 MHz. $\pm\Delta$, then filtered and amplified.


BLOCK DIAGRAM
Lock-on signal to REFERENCE PILOT
F13 : 10 MHz from REFERENCE PILOT.
10 MHz output
F3 : 2 MHz ± Δf
or
F15 : 2 MHz ± Δf
to PHASE-FREQUENCY COMPARATOR
from INTERPOLATOR
Phase - locking
A43
A42
FL 24 10 MHz
FL 25 10 MHz
A44
D14
D14
D15
D14
FL 28 9 MHz
CP8
M7
F14 : 9 MHz
to INTERPOLATOR
D16
A47
FL 26 10 MHz
A46
FL27 4 MHz
A45
1 à 5 - 10 MHz external reference
A48
Output to rear panel
FL 29 0.150kHz
RF
1kHz
FL 30 1kHz
A49
Internal modulating signals to ANALOGUE FRONT PANEL
Output to rear panel
TO PHASE/ FREQUENCY COMPARATOR and CPU
to COUNTERS and Option 05

CONNECTOR PIN-OUT

Internal AF - low frequency modulating signal to Modulations board	1
AF output to rear panel	2
Earthed coaxial socket	3
1 kHz output to rear panel	4
1 kHz - low frequency modulating signal to Modulations board	5
1 kHz TTL-compatible to counters	8
AF Vernier control voltage from register board	12
2 MHz ± Δf from interpolator	13
2 MHz or 2 MHz ± Δf to phase-frequency comparators	15
Internal pilot lock-on	17
Rear panel LED pilot lock-on indicator	19
External lock-on frequency from rear panel	20
9 MHz output to interpolator	34 35
4 MHz output to phase-frequency comparators and CPU	36 37
10 MHz reference frequency from internal pilot	38 39
10 MHz reference output to rear panel	40 41
+ 12 V	44
+ 5 V	45 46
- 12 V	47
⏚ (via mother board)	6 9 14 16 18 21 22 23 25 to 30
Pins not listed not connected	NC

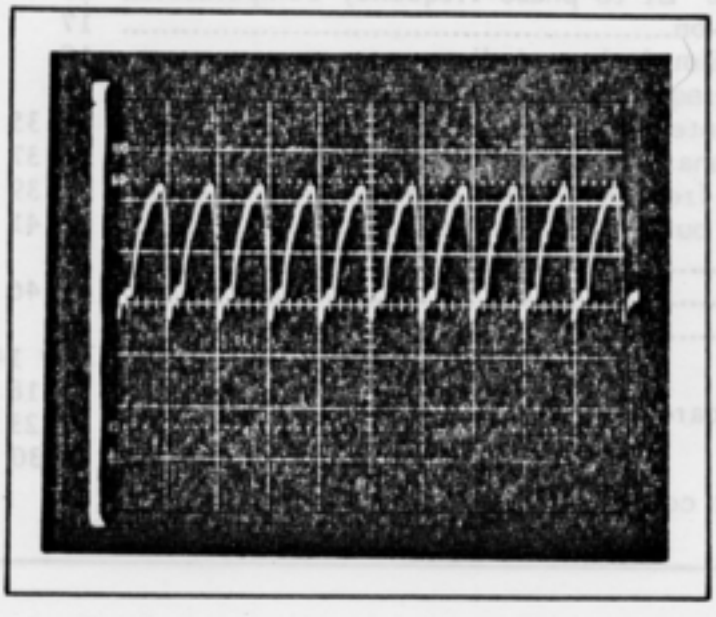
ADJUSTMENTS - BOARD REPAIRED

Required equipment

- Board extender,
- 75 MHz. oscilloscope,
- 20 MHz. wobulator,
- 20 000 digits DVM.

1) 10 MHz. Reference (rear panel)
Connect the oscilloscope to the rear BNC plug then adjust T14 so as to obtain the maximum output level (U = 1,4 Vpp ± 0,3)

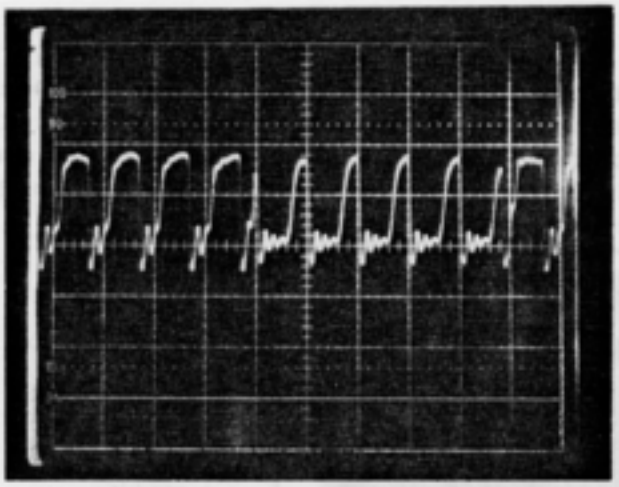
2) 10 MHz. Shaper
Connect the oscilloscope probe across PT6 and adjust T12 so as to obtain the maximum level (U = 500 mVpp ± 75)
Make sure that the level on the collector of Q14 is equal or more than 4 Vpp



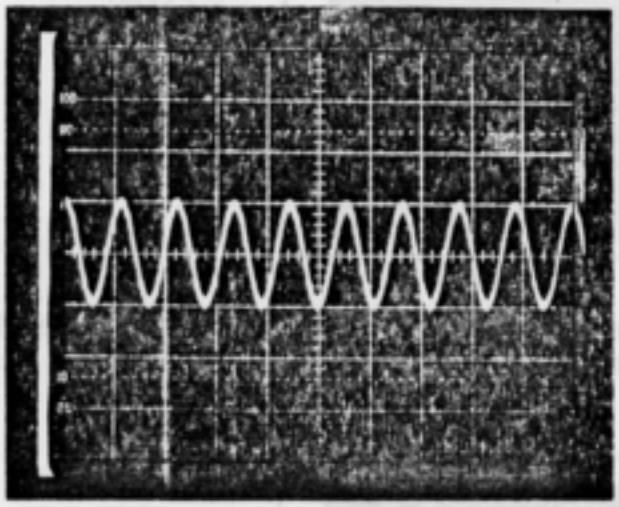
2V/div
0.1 µs/div

3) 4 MHz. Reference
Connect the oscilloscope probe across R36 of the connector and its ground at the pin 37. Adjust T11 so as to obtain a maximum reading (U = 350mVpp ± 50)

4) 9 MHz. Reference
Connect the oscilloscope probe across 34 and 35 (ground) of the connector. Adjust T9 and T10 so as to obtain a maximum reading (U = 200 mVpp ± 20)
Make sure that the frequency is 9 MHz



9 MHz
2V/div
0.1 µs/div



9 MHz output
0.1V/div
0.1 µs/div

5) 1 kHz sinusoidal signal
Connect the voltmeter between the pin 5 of the connector and the ground
Adjust P3 so as to read 3.535V
Make sure that the voltage on the pin 4 is 5 V ± 50 mV)

6) Shaper 12V - 4 MHz
Connect the oscilloscope probe to the collector of Q8
Check the amplitude of the signal "0" : 0.4V ; "1" : 11V.

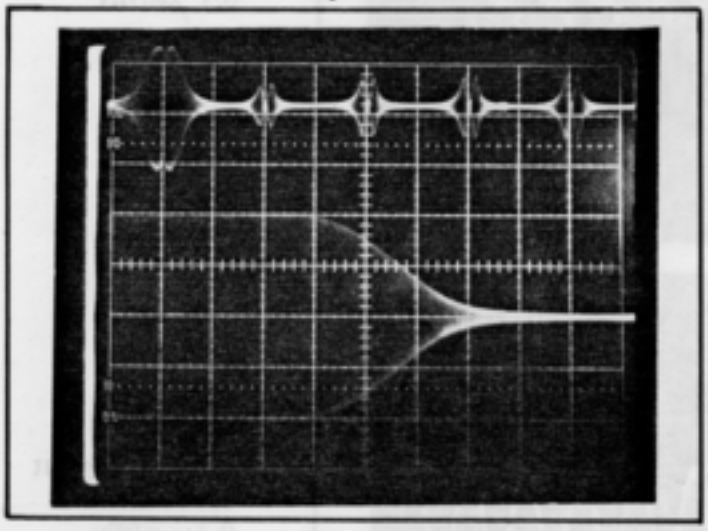
7) 1 kHz. TTL
Connect the oscilloscope probe to PT9 : square signal amplitude :
5 Vpp ± 0.5

8) Switch 2 MHz. or 2 MHz. ± Δ
Connect the oscilloscope probe to 15 of the connector. Switch the Vernier/AF switch to Vernier. Read a 2 MHz. frequency on the scope. Remove the interpolator board connection verify that the signal vanishes. Vernier switch set on "0", a 2 MHz. signal should come back. Switch set on AF : no modification should occur

9) 2 MHz. filter
Connect the oscilloscope probe to PT3. Adjust T4-T5-T6 so as to obtain a maximum reading between 0.7 and 1 V according to P2 setting

10) Mixer, symmetrical amplifier and output filter

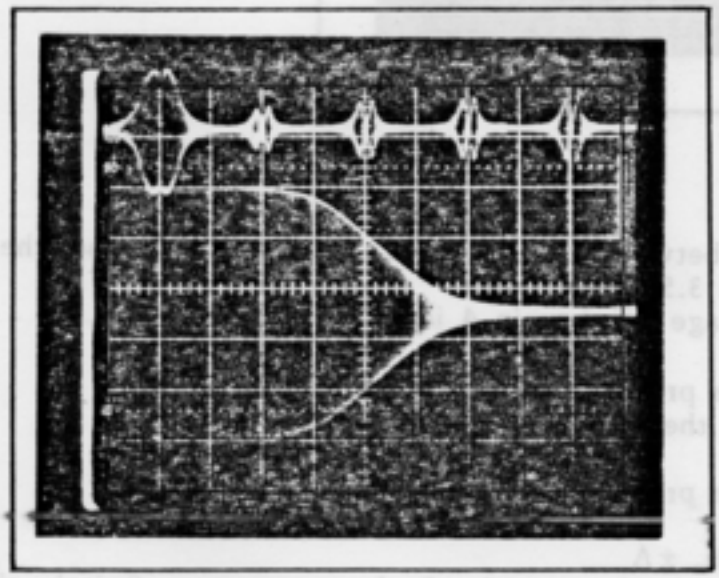
Center the frequency of the wobulator on 12.5 MHz. with a peak F of 2.5 MHz. By means of a coaxial cable loaded by 50 ohms, feed the signal across R76 on the interpolator board ; level 0 dBm. Connect the oscilloscope probe at PT1. Adjust T1-T2-T3 (See oscilloscope patterns). The total real dispersion on the oscilloscope is 1 MHz.



Signal at PT1
0.5V/div
100kHz/div

11) Output amplifier

Connect the probe to the pin "1" of the connector, with a level slightly different from 10 Vpp. Adjust T3 so as the level remain constant whithin the range and up to 350 kHz



2V/div
100kHz/div

12) Cancellation of the residual DC voltage

Disconnect the wobulator source, connect a DC DVM to the pin "1" of the connector. Adjust P1 so as to obtain the minimum voltage, 0V ± 2 mV. Same adjustment to be carried-out on the pin "2" of the connector

13) Output level adjust

a) Display a 1000 Hz. AF. Adjust P2 so as to read 3.535 V on the pin 1 of the connector

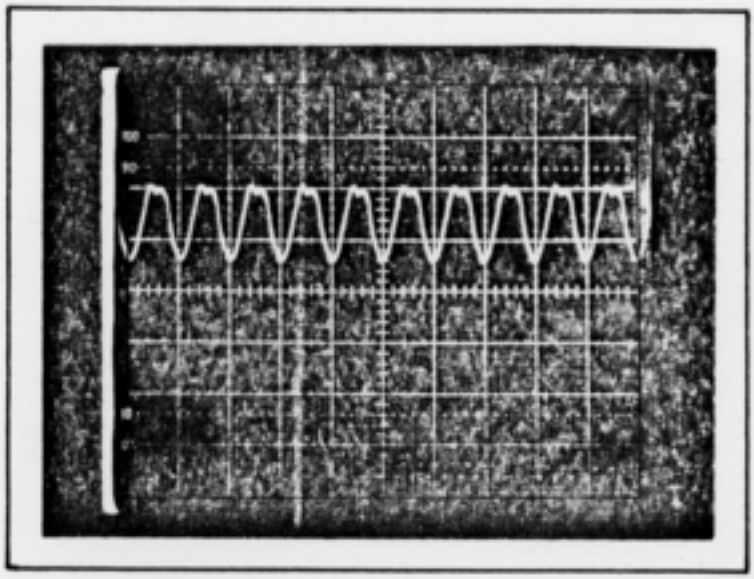
b) Make sure that 5 V ± 50 mV. can be obtained at the pin "2"

14) 10 MHz. Filter

Connect the wobulator, output level - 10 dBm. centered on 10 MHz. to the BNC socket labelled "Phase lock". Connect the probe of the oscilloscope to PT5. Adjust T7 and T8 so as to center the filter on the 10 MHz. marker. Passband at 3 dBm : around 250 kHz. Output level = 0.7 Vpp. ± 0.15. Check the sub-harmonics of the filter up to 1 MHz.

15) External 10 MHz. shaper

On the wobulator, display 10 MHz. CW. Connect the probe of the oscilloscope to the collector of Q11. Ascertain that the Peak to peak amplitude is equal or more than 4.5 V. Display 1 MHz. The signal amplitude must remain the same.



Signal at PT5
0.5V/div
0.1 s/div

16) Phase locking voltage of the pilot

Verify, in feeding a 10 MHz. frequency ± 15 Hz. that the amplitude of the beat frequency is more than 11 Vpp

PHASE-FREQUENCY COMPARATORS

The CPF subsystem comprises part of the phase-lock loop generating the output frequency 500 Hz steps, the phase-frequency comparators, and the alarm and disable circuits associated with the 300/670 MHz and 320/650 MHz oscillators.

The 500 Hz steps are generated by means of an oscillator covering the range from 32 to 42 or from 58 to 48 MHz, according to whether the 20/25 MHz signal is carrying the direct or inverted form of the 1 kHz steps (relative to the output frequency). The output signal from this oscillator is input to the counter subsystem where it is divided by 32 000 to 58 000 and compared with a 1 kHz reference frequency from the timebase. It is also successively divided by 2 (integrated circuit SN1) and mixed with the 20-25 MHz signal from the 20/25 MHz oscillator module. The difference frequency is selected by a bandpass filter which thus outputs a frequency of 4 MHz. This is divided by 8 in integrated circuit SN3 and compared with a reference frequency obtained by dividing the 2 MHz or 2 MHz ± Δf output from the timebase by 4 in integrated circuit SN6. The comparison of these two frequencies is the basis for locking the 32/42 MHz or 58/48 MHz oscillator, range switching being provided by the parallel connection of inductor T2 and capacitor C11 (12pF) across its tuned circuit. The phase-frequency comparator providing this phase locking action assures also a modulation phase in DC of the output signal.

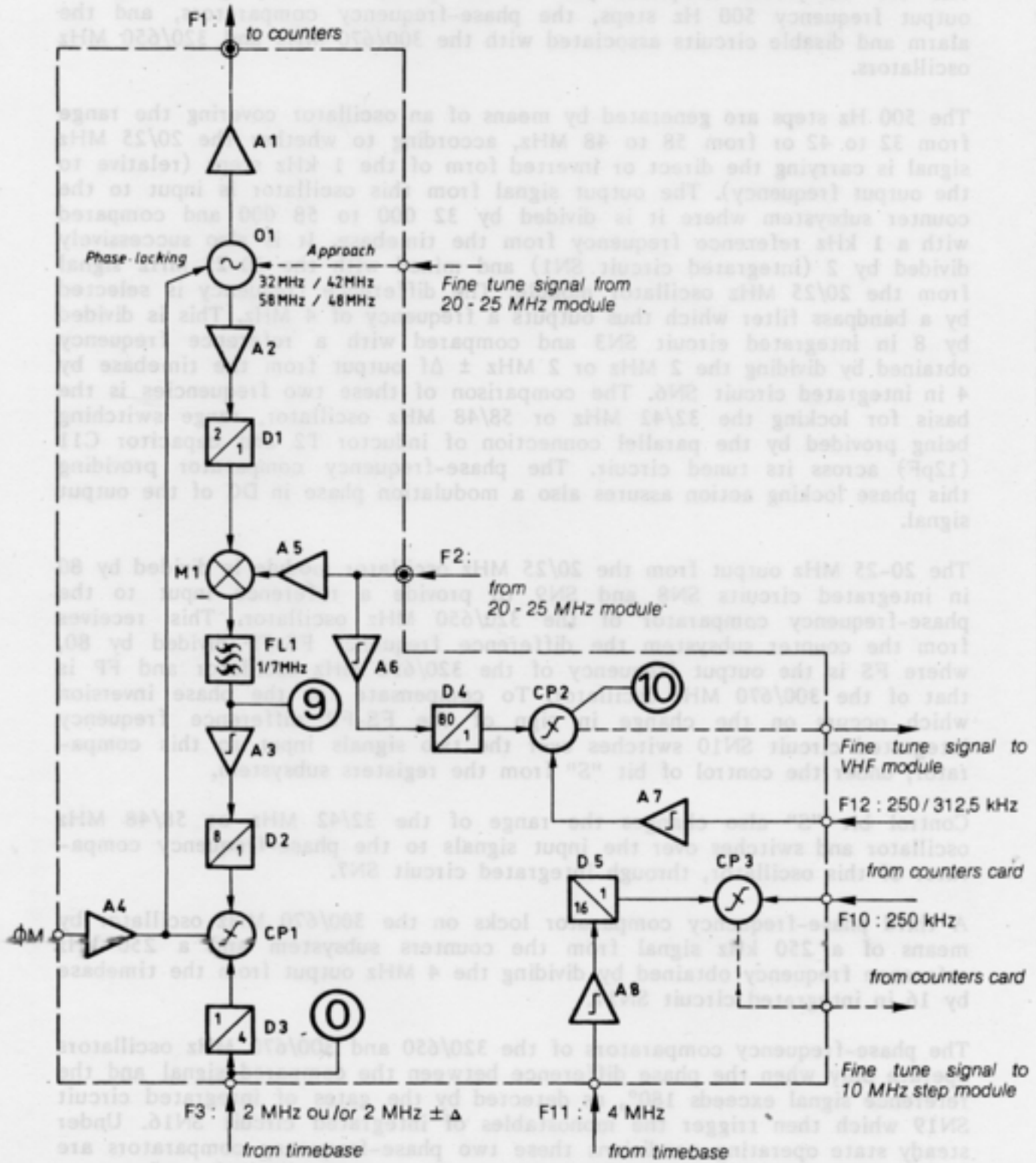
The 20-25 MHz output from the 20/25 MHz oscillator module is divided by 80 in integrated circuits SN8 and SN9 to provide a reference input to the phase-frequency comparator of the 320/650 MHz oscillator. This receives from the counter subsystem the difference frequency FS-FP divided by 80, where FS is the output frequency of the 320/650 MHz oscillator and FP is that of the 300/670 MHz oscillator. To compensate for the phase inversion which occurs on the change in sign of the FS-FP difference frequency integrated circuit SN10 switches over the two signals input to this comparator, under the control of bit "S" from the registers subsystem.

Control bit "S" also changes the range of the 32/42 MHz or 58/48 MHz oscillator and switches over the input signals to the phase-frequency comparator of this oscillator, through integrated circuit SN7.

A third phase-frequency comparator locks on the 300/670 MHz oscillator by means of a 250 kHz signal from the counters subsystem and a 250 kHz reference frequency obtained by dividing the 4 MHz output from the timebase by 16 in integrated circuit SN17.

The phase-frequency comparators of the 320/650 and 300/670 MHz oscillators operate only when the phase difference between the compared signal and the reference signal exceeds 180°, as detected by the gates of integrated circuit SN19 which then trigger the monostables of integrated circuit SN16. Under steady state operating conditions these two phase-frequency comparators are inactive, the 320/650 and 300/670 MHz oscillators being locked on by sampling type phase comparators in the VHF and 10 MHz steps modules, respectively.

BLOCK DIAGRAM



CONNECTOR PIN-OUT

Phase modulation (ØM = from analogue front panel)	1
Test : 4 MHz level to registers board	2
Test : 2 MHz or 2 MHz ± Δf level to registers board	3
Fine tune signal from 20-25 MHz module (lock-on voltage)	6
2 MHz or 2 MHz ± Δf from timebase	15
Fined tune signal FP* to 10 MHz step module	24
Fine tune voltage FS* to interface module	31
Fine loop disable and fine tune FP enable to 10 MHz step module	32
Fine loop disable and fine tune FS enable to registers and interface boards	33
Polarity bit (1)	34
Change of polarity bit (1)	35
4 MHz from timebase	36 37
250 kHz from counters board	38
FS-FP/80 from counters board	40
Polarity of FS-FP/80 from counters board	41
+ 18 V	42
+ 12 V	44
+ 5 V	45 46
- 12 V	47
⏚	16 21 22 23
Pins not listed not connected	NC

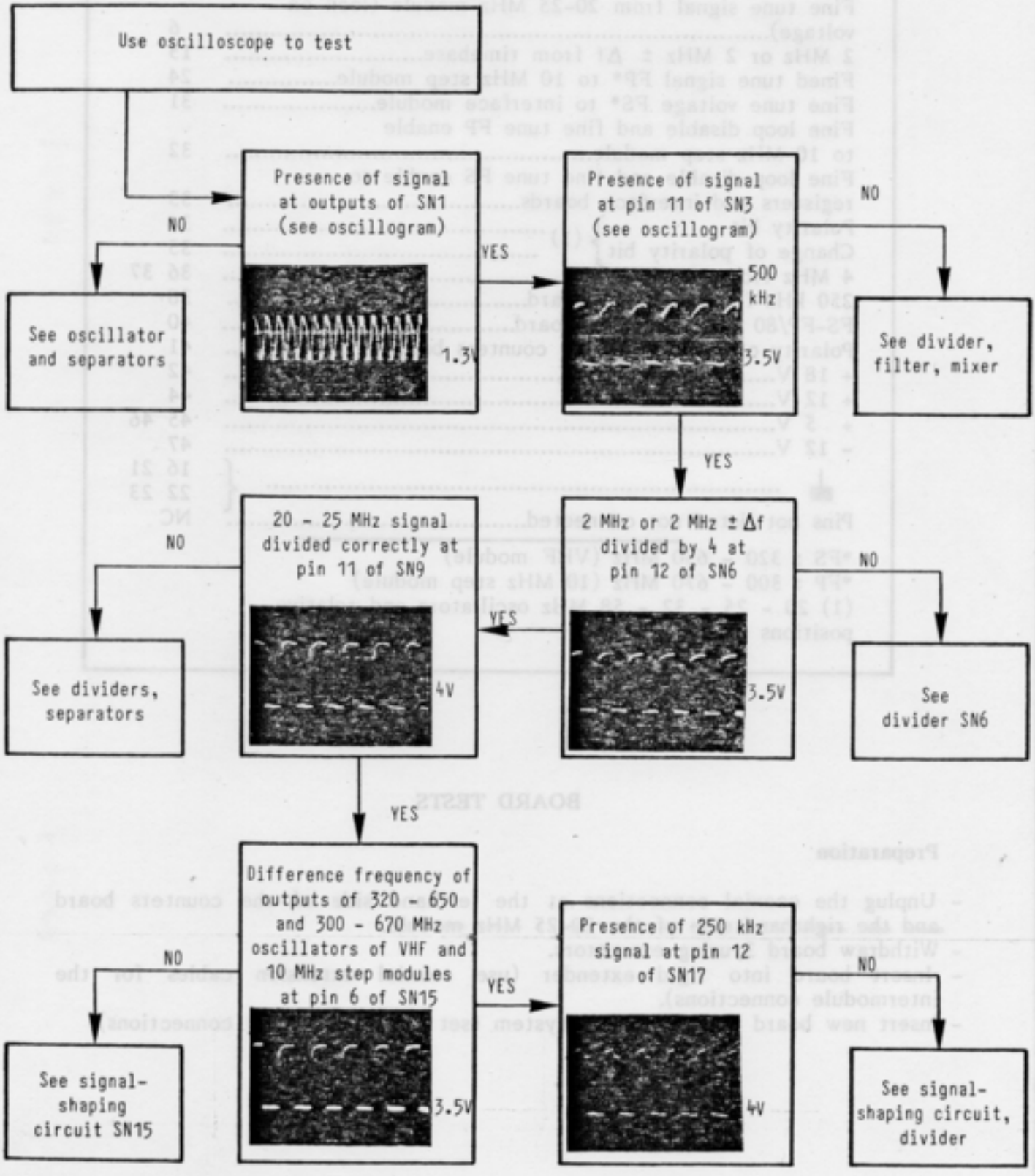
*FS : 320 - 650 MHz (VHF module)
*FP : 300 - 670 MHz (10 MHz step module)
(1) 20 - 25 - 32 - 58 MHz oscillators and relative positions of FS and FP

BOARD TESTS

Preparation

- Unplug the coaxial connections at the lefthand side of the counters board and the righthand side of the 20-25 MHz module.
- Withdraw board 3 using extractors.
- Insert board into rigid extender (use coaxial extension cables for the intermodule connections).
- Insert new board if replacing-subsystem (set up again coaxial connections).

TROUBLESHOOTING CHART



ADJUSTMENTS

BOARD REPAIRED

Equipment required :
- 75 MHz oscilloscope,
- frequency meter,
- multimeter,
- wobbulator,
- Subclic Tee connector.

1) 20 - 25 MHz input circuit

a) Apply to "20-25 MHz" Subclic input connector a signal swept from 20 - 25 MHz at 60 Hz and 0 dBm level
b) Short-circuit the common point of R2/Q1 emmitter to the transistor case
c) Connect the oscilloscope to PT08 and adjust T6 to centre the resonance peak on 22.5 MHz, at level 0.7 Vpp ± 80 mV
d) Remove the short-circuit

2) 29.6 - 60.4 MHz oscillator

a) Connect Tee connector to 29.6 - 60.4 MHz Subclic output to enable coaxial connection to counters board and fitting of BNC adaptator
b) Connect the BNC adaptator to the frequency meter to which the generator is locked on
c) Set 354.990 MHz on the generator and verify that the frequency meter reads 41.980 MHz
d) Connect the multimeter to PT1 and adjust T1 to obtain a level of 11.5 V
e) Set 355 MHz (frequency meter reading 58 MHz). Adjust T2 to obtain a level of 11 V at PT1
f) Set 350 MHz (frequency meter reading 32 MHz). Verify that the level at PT1 is 3.5 V ± 0.25 V
g) Set 349.990 MHz (frequency meter reading 48.020 MHz). The level at PT1 should be 3.5 V ± 0.25 V

3) Continuous FM at 300 kHz

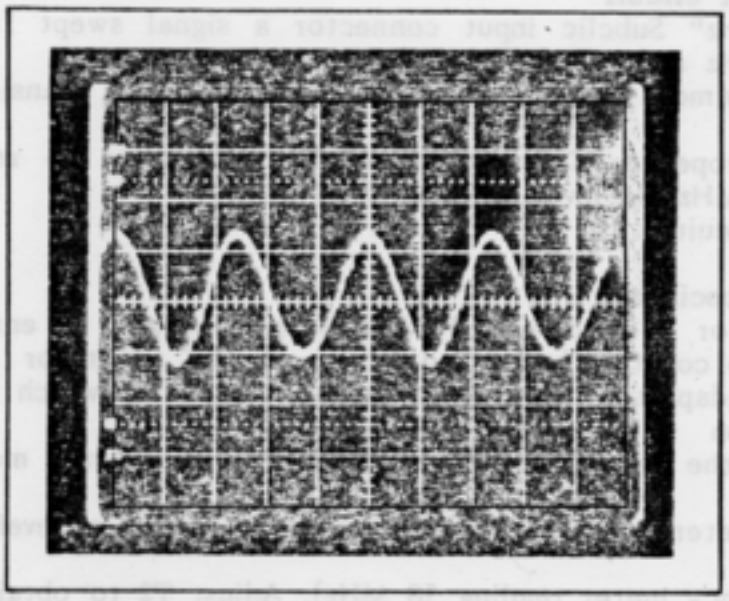
a) Connect the oscilloscope to PT5 and PT6. Adjust P1 to obtain the same peak amplitude on both channels
b) Set 100 MHz and enable FM modulation (DC coupling). Select the 300 kHz range and rotate the modulation depth potentiometer fully clockwise
c) Apply input voltage of 4.24 V to FM input and check that the frequency indicated increases by 300 kHz
d) Sweep across the 100 - 102.5 MHz band and check that the peak amplitude variation is not more than 0.2 s. Reverse the input polarity and repeat the above test from 102.5 to 100 MHz.

4) Continuous ØM

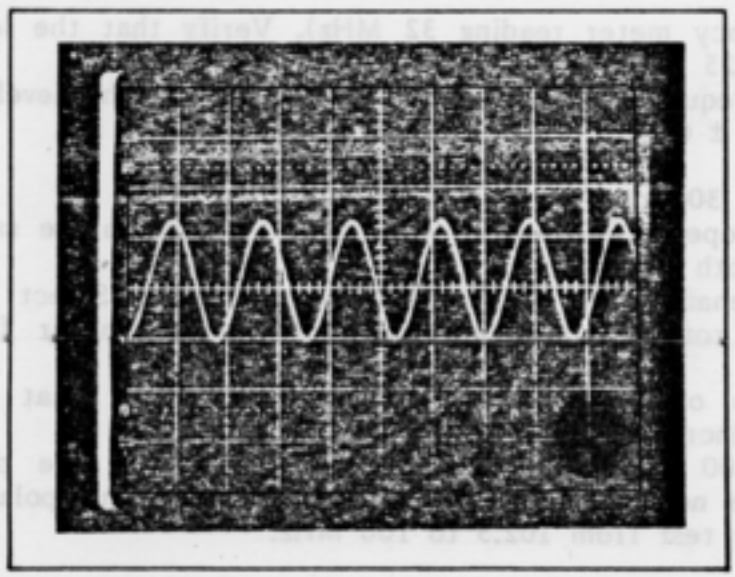
a) Set 350 MHz and select phase modulation (ØM)
b) Check voltage at connector pin 1 is 1.06 V
c) Connect the oscilloscope to PT5 and PT6
d) Sweep the 350 - 355 MHz band in steps of 10 kHz and adjust P2 to obtain a mean peak amplitude of 0.24 s

4) Continuous ØM

a) Set 350 MHz and select phase modulation (ØM)
b) Check voltage at connector pin 1 is 1.06 V
c) Connect the oscilloscope to PT5 and PT6
d) Sweep the 350 - 355 MHz band in steps of 10 kHz and adjust P2 to obtain a mean peak amplitude of 0.24 s



4 MHz reference board output
100ns/div
100mV/div



32 - 58 MHz output
10ns/div
0.2V/div

COUNTERS

This subsystem comprises the 32 000 to 58 000 counter and the phase-frequency comparator of the phase-lock loop used to generate the 500 Hz steps, the 30 to 67 counter of the loop used to generate the 10 MHz steps and the circuits forming the FS-FP/80 difference signal and determining its polarity.

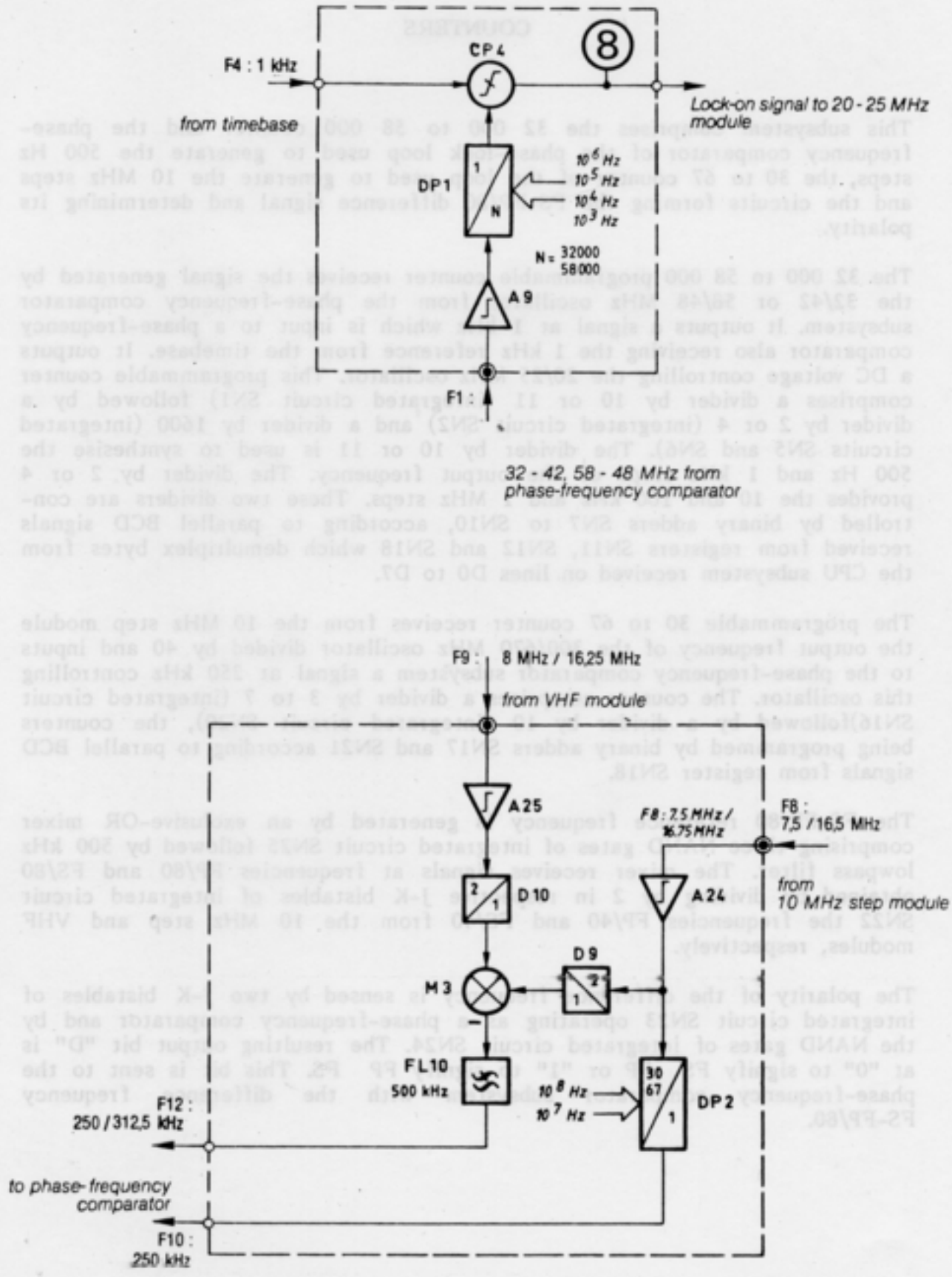
The 32 000 to 58 000 programmable counter receives the signal generated by the 32/42 or 58/48 MHz oscillator from the phase-frequency comparator subsystem. It outputs a signal at 1 kHz which is input to a phase-frequency comparator also receiving the 1 kHz reference from the timebase. It outputs a DC voltage controlling the 20/25 MHz oscillator. This programmable counter comprises a divider by 10 or 11 (integrated circuit SN1) followed by a divider by 2 or 4 (integrated circuit SN2) and a divider by 1600 (integrated circuits SN5 and SN6). The divider by 10 or 11 is used to synthesise the 500 Hz and 1 kHz steps of the output frequency. The divider by 2 or 4 provides the 10 and 100 kHz and 1 MHz steps. These two dividers are controlled by binary adders SN7 to SN10, according to parallel BCD signals received from registers SN11, SN12 and SN18 which demultiplex bytes from the CPU subsystem received on lines D0 to D7.

The programmable 30 to 67 counter receives from the 10 MHz step module the output frequency of the 300/670 MHz oscillator divided by 40 and inputs to the phase-frequency comparator subsystem a signal at 250 kHz controlling this oscillator. The counter comprises a divider by 3 to 7 (integrated circuit SN16)followed by a divider by 10 (integrated circuit SN20), the counters being programmed by binary adders SN17 and SN21 according to parallel BCD signals from register SN18.

The FS-FP/80 reference frequency is generated by an exclusive-OR mixer comprising three NAND gates of integrated circuit SN25 followed by 500 kHz lowpass filter. The mixer receives signals at frequencies FP/80 and FS/80 obtained by dividing by 2 in respective J-K bistables of integrated circuit SN22 the frequencies FP/40 and FS/40 from the 10 MHz step and VHF modules, respectively.

The polarity of the difference frequency is sensed by two J-K bistables of integrated circuit SN23 operating as a phase-frequency comparator and by the NAND gates of integrated circuit SN24. The resulting output bit "D" is at "0" to signify FS FP or "1" to signify FP FS. This bit is sent to the phase-frequency comparator subsystem with the difference frequency FS-FP/80.

BLOCK DIAGRAM



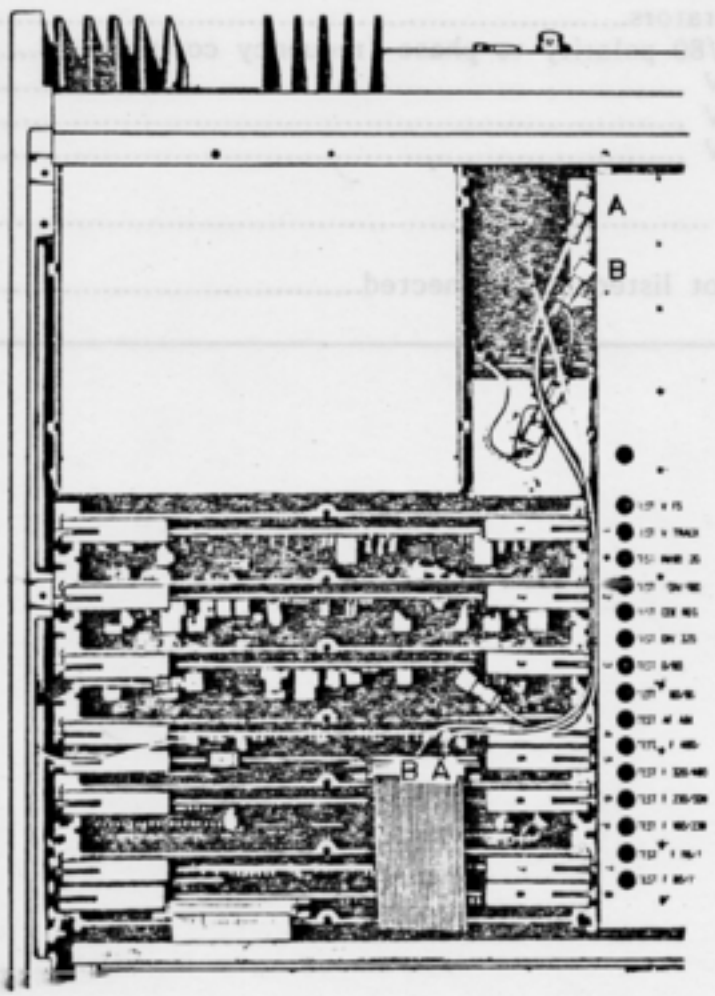
CONNECTOR PIN-OUT

Test : 1 kHz lock-on to registers board		4
80/100 Hz oscillator lock-on to 20 - 25 MHz module		6
1 kHz ⊓⊔ reference from timebase		8
Internal data bus CPU board I/O s	D0	13
	D1	14
	D2	15
	D3	16
	D4	17
	D5	18
	D6	19
	D7	20
1 MHz ⊓⊔(E) from CPU board		24
Internal address bus Inputs from CPU board	A0	26
	A1	27
	A2	28
	A3	29
	A4	30
250 kHz to phase-frequency comparators		38
FS-FP/80 difference frequency to phase-frequency comparators		40
FS-FP/80 polarity to phase-frequency comparators		41
+ 12 V		44
+ 5 V		45 46
- 12 V		47
⏚		9 21 22 23 25 34 39
Pins not listed not connected		NC

BOARD TESTS

Fitting board to extender and replacing board :

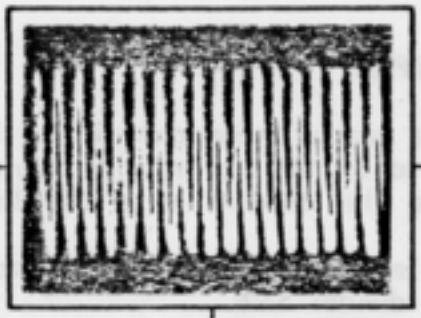
- Disconnect the lefthand coaxial connection to board 3 (phase-frequency comparators)
- Remove the connections from the relay board behind the pilot frequency module, to release the coaxial connections attached to the counters board
- Pull board 5 halfway out, to avoid damaging capacitor C17 on withdrawing the counters board
- Withdraw board 4 using extractors and insert into rigid extender
- If replacing the subsystem, insert the new board
- and
  * replace board 5
  * replace lefthand coaxial connection on board 3
  * replace coaxial connections on relay board



TROUBLESHOOTING CHART

Use oscilloscope to test

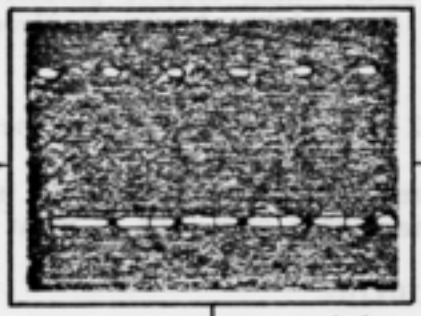
Signal at between 32 and 58 MHz on pin 16 of SN1 (see oscillogram 1)



1.1 V

See input signal-shaping circuit

32 000 to 64 000 counter output signal at pin 3 of SN14 (see oscillogram 2)



4.6 V

See 32 000-64 000 counter

FP/40 signal at pin 12 of SN22 (see oscillogram 3)

3.5 V

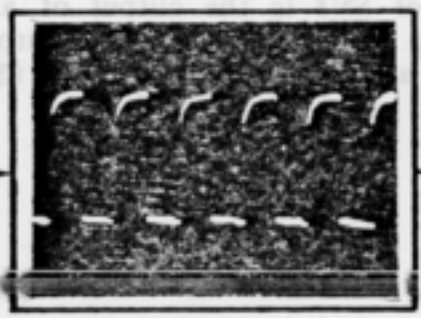
See input signal-shaping circuit or divider (SN22)

FS/40 signal at pin 9 of SN22 (see oscillogram 4)

3.5 V

See input signal-shaping circuit or divider (SN22)

250 kHz signal at pin 12 of SN20 (see oscillogram 5)



4 V

See 30 - 60 counter

32 000 - 64 000 COUNTER

This counter divides the output frequency of the 32/58 MHz oscillator on the CPF board by 32 000 to 58 000 to input a signal at 1 kHz to comparator CP4 which phase-locks the 80-100 MHz oscillator (20-25 MHz following division by 4).
The counter comprises an input divider SN1, two intermediate dividers SN2 and SN5 and an output divider SN6.
The dividing ratio is controlled by NAND circuits SN3 and SN4 and adders SN10, SN09, SN08 and SN07 which receive parallel BCD signals from registers SN11 and SN12 which demultiplex bytes received from the CPU subsystem over lines D0 to D7.

The minimum ratio (32 000) is provided by the following direct-connected configuration :
- SN1 divides by 10 when at least one input PE is at "1"
- SN2 divides by 2 when input "K" (pin 3) is at "0"
- SN5 divides by 16,
- SN6 divides by 100 (10x10).

This minimum ratio is obtained when logic "1" is applied to each input of adders SN7 to SN10. This is the case when the generator output frequency is a multiple of 10 MHz in the range 320 - 650 MHz.

Operation of the counter may be tested using the data set out below. The principal divider signals are marked A to E on the electronic circuit diagram.
A : ECL input signal
DC level $\simeq$ 3.7 V
RF level $\simeq$ 1 Vpeak
B : Squarewave signal, TTL level
C : Squarewave signal, TTL level
D : TTL-compatible pulse signal with 0.25 cyclic ratio (low), increased to CMOS-compatible level by load resistor R11
E : CMOS-compatible pulse signal with 0.20 cyclic ratio (high).

SETTING THE DIVISION RATIO

a) Entry of units digits

The input divider SN1 divides by 11 when both inputs PE (signals J and H) are at logic "0".

Signal J at the output of SN3 is the output of an NAND gate receiving the output of SN2 (dividing by 2 or 4) and the output of SN5 (dividing by 16) and the "D" output of a counter dividing by 10 (1/2 SN6).

The cyclic ratio of negative pulse J is thus 20/x where "x" represents the division ratio variation of the output divider formed by SN2, SN5 and SN6.

Signal I is the carry output from adder SN10. When the input carry is "1" (pin 9) this is a negative-going pulse with a cyclic ratio of N/10. The ratio is (N + 1)/10 when the input carry is "0". N represents the units applied to the inputs of SN10.

The input carry corresponds to the half-unit P ANDedwith signal K, the cyclic ratio of which is 50%.

The main cyclic ratio is thus (N + P/2)/10.

When I is ANDed with signal J in SN1 the cyclic ratio becomes 2 (N + P/2)/x :
- the division ratio is 10 when I + J = 1
  for example : x - 2 (N + P/2times)
- the division ratio is 11 when I + J = 0
  for example : 2(N + P/2times)

The actual cyclic ratio is :

$$\boxed{10\,[x - 2(N + P/2)] + 11[2(N + P/2)]}$$

This expression reduces to 10 x 2N + P (1)
where the action of N and P is independent of the value of x.

b) Entry of tens, hundreds and thousands digits

Intermediate stage SN2 divides by 4 when its input "K" (pin 3) is at logic "1", in other words when signal H from the adder circuits is low. Signal H corresponding to the output carry of SN7 has a cyclic ratio M/1600, the division ratio of SN2 being 4 for M pulses and 2 for the other 1600-M pulses.

The division ratio of the output divider (SN2, SN5, SN6) is thus :

$$x = 4M + 2(1600-M) = 3200 + 2M$$

The value of x thus determined is introduced into expression (1) to obtain the overall division ratio :

$$T = 10(3200 + 2M) + 2N + P$$
$$T = 32000 + 2(10M + N + P/2)$$

Note that the overall division ratio may vary between 32000 and 63999, whereas only the ranges 32000 to 41999 and 48001 to 58000 are used.

REGISTERS

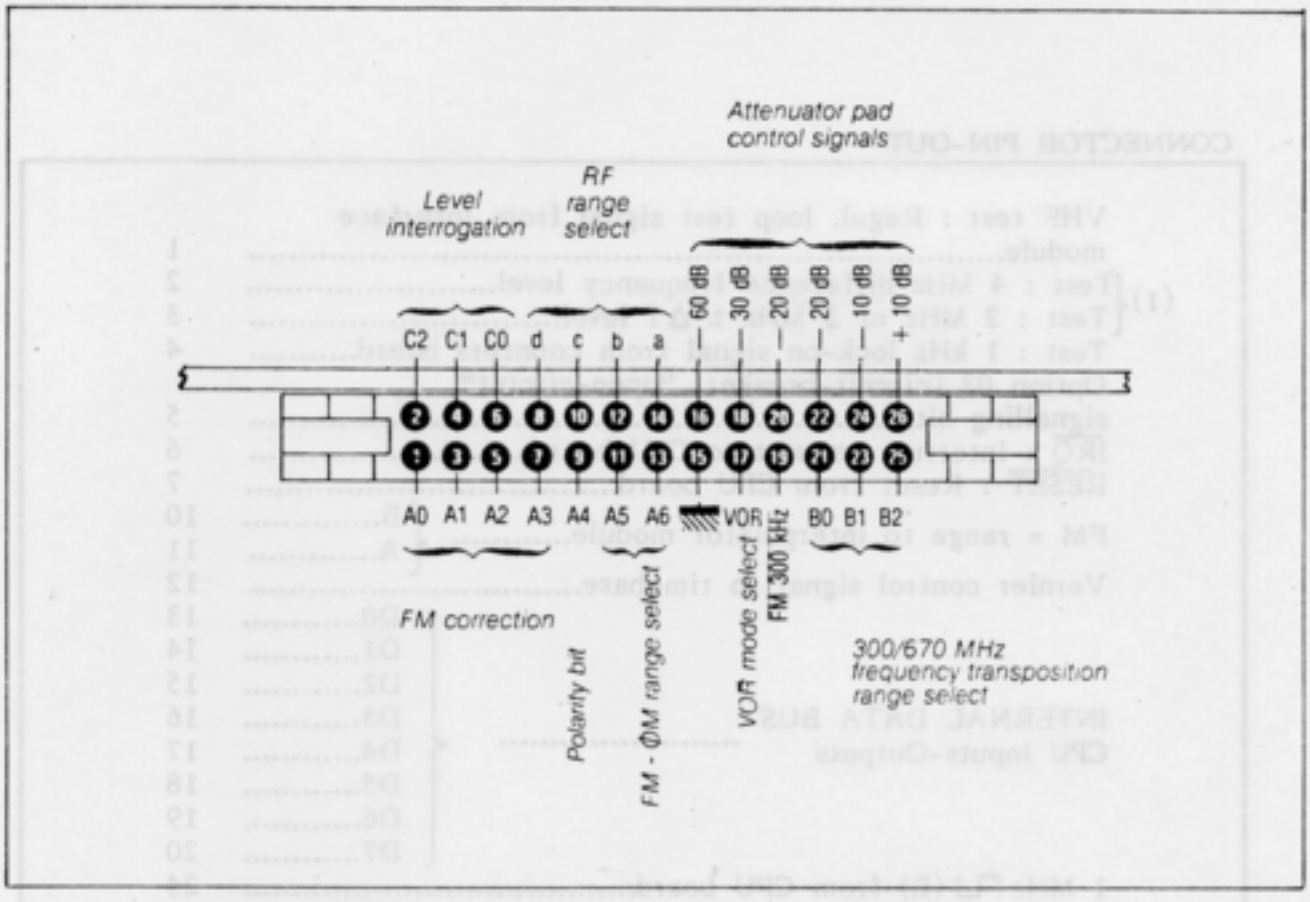
CONNECTOR PIN-OUT

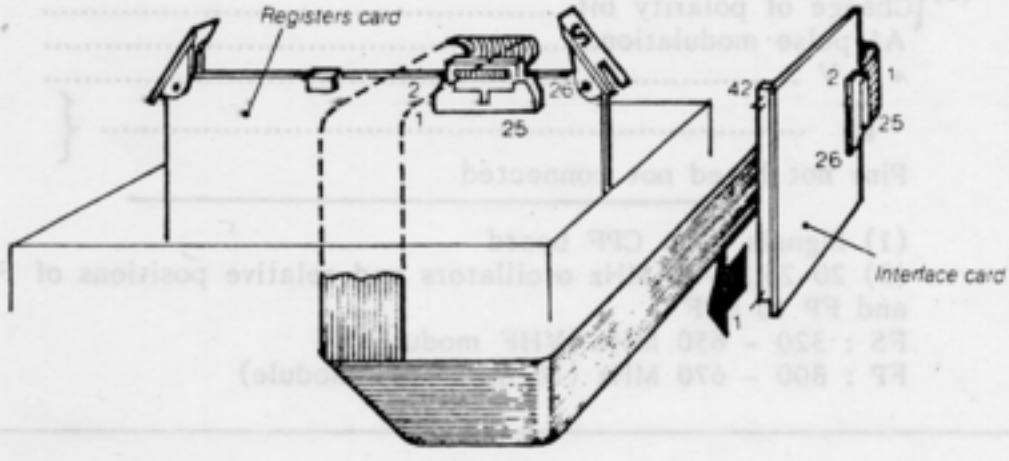
	VHF test : Regul. loop test signal from interface module	1
(1)	Test : 4 MHz difference frequency level	2
(1)	Test : 2 MHz or 2 MHz ± Δf level	3
	Test : 1 kHz lock-on signal from counters board	4
	Option 02 (circuit-breaker) "open-circuit" signalling bit	5
	$\overline{IRQ}$: Interrupt request to CPU board	6
	$\overline{RESET}$: Reset from CPU board	7
	FM = range to interpolator module — B	10
	FM = range to interpolator module — A	11
	Vernier control signal to timebase	12
	INTERNAL DATA BUS CPU Inputs-Outputs — D0	13
	D1	14
	D2	15
	D3	16
	D4	17
	D5	18
	D6	19
	D7	20
	1 MHz ⊓⊔ (E) from CPU board	24
	INTERNAL ADDRESS BUS Inputs from CPU board — A0	26
	A1	27
	A2	28
	A3	29
	A4	30
	Fine loop disable and fine tune FS enable from phase-frequency comparators	35
(2)	Polarity bit	36
(2)	Change of polarity bit	37
	A1 pulse modulation	40 41
	+ 5 V	45 46
	⊥	21 22
	⊥	23 25

Pins not listed not connected

(1) Signals from CPF board
(2) 20-25,32-58 MHz oscillators and relative positions of FS and FP to CPF
FS : 320 - 650 MHz (VHF module)
FP : 300 - 670 MHz (10 MHz step module)

INTERFACE BOARD CONNECTOR PIN-OUT





BOARD TESTS

PREPARATION

Fitting board to extender or replacing the board :
- Disconnect the connecting wires from the interface board
- Remove board 5 using extractors
- Fit to extender to carry out tests and connect connecting wires
- If replacing the subsystem insert the new board and connect connecting wires. No adjustments are required to ensure board/instrument compatibility.

TROUBLESHOOTING
OPERATING TEST

1) Interpolator and FM/ØM ranges

a) Set any output frequency and level
b) Disable the frequency Vernier control
c) Select external FM source with DC coupling Apply LF modulating signal to FM input
d) Select positions PM, FM3, FM30 and FM300 successively, testing the logic state at points 10, 11, 12 A5 and A6 (of 47 points connector)

Check / Enable	10	11	12	A6	A5
PM	0	0	0	0	0
FM3	0	1	1	0	1
FM30	1	1	1	1	1
FM300	1	0	1	1	0

2) FM correction

a) Set frequency 330 MHz and 100 kHz step resolution
b) Set the frequencies shown in the table below successively using the manual increment pushbutton (+) on the front panel. Verify the logic states at points A0, A1, A2 and A3.

MHz	A0	A1	A2	A3
330	0	0	0	0
330.2	1	0	0	0
330.4	0	1	0	0
330.8	1	1	0	0
331.2	0	0	1	0
331.6	1	0	1	0
332	0	1	1	0
332.4	1	1	1	0
332.9	0	0	0	1
333.2	1	0	0	1
333.6	0	1	0	1
334	1	1	0	1
334.4	0	0	1	1
334.6	1	0	1	1
334.8	0	1	1	1

3) Polarity

Polarity bit A4 changes state every 5 MHz :
Set 320 MHz and check logic state at point A4 = 0
Set 335 MHz and check logic state at point A4 = 1
Set 340 MHz and check logic state at point A4 = 0

4) RF ranges

a) Select CW mode
b) Set the frequencies indicated in the table below successively and test the logic state at points a, b, c and d.

MHz	d	c	b	a
1	0	1	1	0
60	1	1	1	0
80	0	0	0	0
115	1	0	0	0
160	0	0	0	1
230	1	0	0	1
320	0	0	1	0
460	1	0	1	0

5) 300/670 MHz oscillator transposition ranges

a) Select CW mode
b) Set the frequencies indicated in the table below successively and test the logic state at points B0, B1 and B2.

MHz	B0	B1	B2
330	0	0	0
400	1	0	0
480	0	1	0
550	1	1	0
640	0	0	1

6) VOR modulation

a) Select amplitude modulation (AM) and position = (DC coupling)
Check that the logic state at point + VOR - is 0
b) Select position VOR and check that the corresponding logic state is 1

7) FM modulation - 300 kHz deviation

a) Select frequency **modulation** (FM) and "300 K" deviation
b) Check that point **FM 300 K** is at logic 0 in the range 80 to 320 MHz
c) Check that point FM 300 K is at logic 1 in the range 320-650 MHz and 0.3 at 80 MHz

8) Attenuator

Select all 10 dB steps from + 20 to - 130 dBm and test logic state at + 10, - 10, - 20, - 20, - 30 and - 60

dB	-60	-30	-20	-20	-10	+10
+20	0	0	0	0	0	1
+10	0	0	0	0	0	0
0	0	0	0	0	1	0
-10	0	0	0	1	0	0
-20	0	0	1	0	1	0
-30	0	1	0	0	1	0
-40	0	0	1	1	1	0
-50	0	1	0	1	1	0
-60	1	0	0	0	1	0
-70	0	1	1	1	1	0
-80	1	0	0	1	1	0
-90	1	1	0	0	1	0
-100	1	0	1	1	1	0
-110	1	1	0	1	1	0
-120	1	1	1	1	0	0
-130	1	1	1	1	1	0

9) Test

a) Press the self-test enabling pushbutton
b) Provoke an "interrupt" by rotating the frequency spinwheel
c) Select resolution step position 0
d) Enable tests 00 to 07 and verify corresponding logic state at points C0, C1 and C2

Test	C2	C1	C0
00	⎍	0	0
01	1	0	0
02	⎍	0	1
03	1	0	1
04	⎍	1	0
05	1	1	0
06	⎍	1	1
07	1	1	1

MICROPROCESSOR

CONNECTOR PIN-OUT

"Power supply present" signal from rectifier board.....		4
$\overline{IRQ}$: Interrupt request from option 004, Front Panel, registers and logic board.....		6
$\overline{RESET}$: To Front Panel, IEEE and registers board.....		7
1 kHz ⊓⊔ from timebase.....		8
2.5 MHz ± Δf from interpolator module.....		12
INTERNAL DATA BUS Counters, registers, front panel and 004 option	D0.....	13
	D1.....	14
	D2.....	15
	D3.....	16
	D4.....	17
	D5.....	18
	D6.....	19
	D7.....	20
1 MHz ⊓⊔ ($\overline{E}$) to counters, registers, front panel and 004 option		24
INTERNAL ADDRESS BUS Outputs to counters, registers front panel and 004 option	A0.....	26
	A1.....	27
	A2.....	28
	A3.....	29
	A4.....	30
	A5.....	31
	A6.....	32
R/$\overline{W}$ (read/write) : 004 option I/0 s		33
4 MHz from timebase.....		36
+ 12 V pilot.....		43
+ 12 V		44
+ 5 V		45 46
- 12 V		47
⏚		9 10 11 21 22 23 34 37
Pins not listed not connected.....		NC

BOARD TESTS

PREPARATION

Fitting board to extender or replacing board :
- Remove connecting wires from registers board (5)
- Withdraw board 6 using extractors
- Fit to extender to carry out tests (connect connecting wires)
- If replacing the subsystem insert the new board and connect the connecting wires

TROUBLESHOOTING
OPERATION CHECK

Equipment required
- Multimeter
- Oscilloscope

1) - 5 V supply :
Check regulator SN15 bottom pin output : - 5 V + 0.25 V

2) + 5 V supply :
Check presence of + 5 V ± 0.25 V on pin 35 of SN1

3) 4 MHz clock :
Connect oscilloscope to pin 11 of SN2 and adjust T1 to obtain maximum level (> 500mVpp)

4) Microprocessor :
a) Don't select RF 1 kHz or AF
b) Check that red indicator lamp top left on board flashes, after each front panel control is operated (frequency spinwheel, keyboard)
c) Enable the frequency resolution 1 kHz and check that the lamp flashes faintly at approximately 4 Hz

5) Interrupted operation :
a) Switch the generator to standby for a few seconds and then re-enable operation, checking that the frequency indicated is the same as that before selecting standby
b) Check that the frequency indicated is the same after disconnecting the mains supply for approximately one second

MODULATIONS BOARD

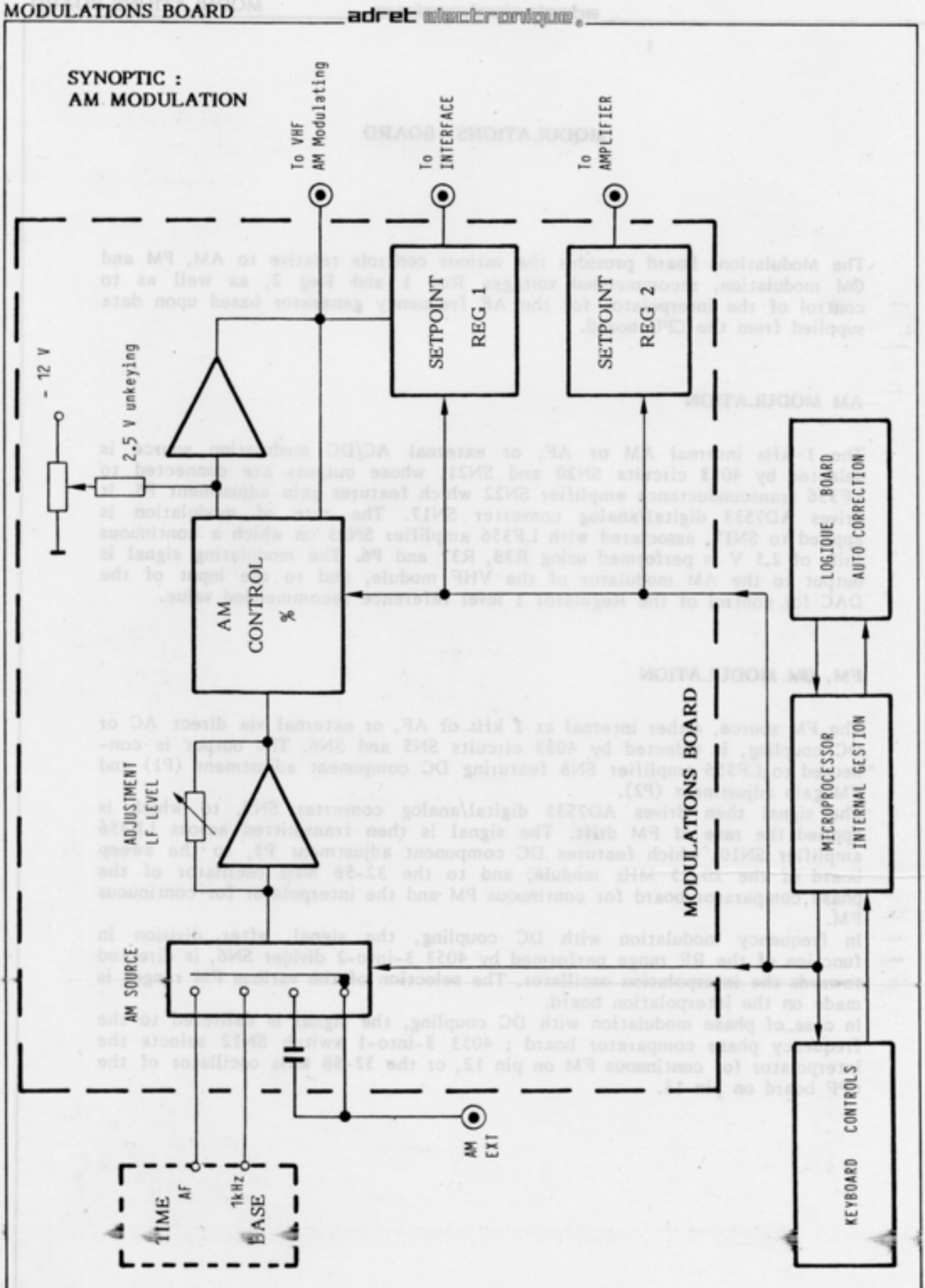
The Modulations board provides the various controls relative to AM, PM and ØM modulation, recommended voltages Reg 1 and Reg 2, as well as to control of the interpolator for the AF frequency generator based upon data supplied from the CPU board.

AM MODULATION

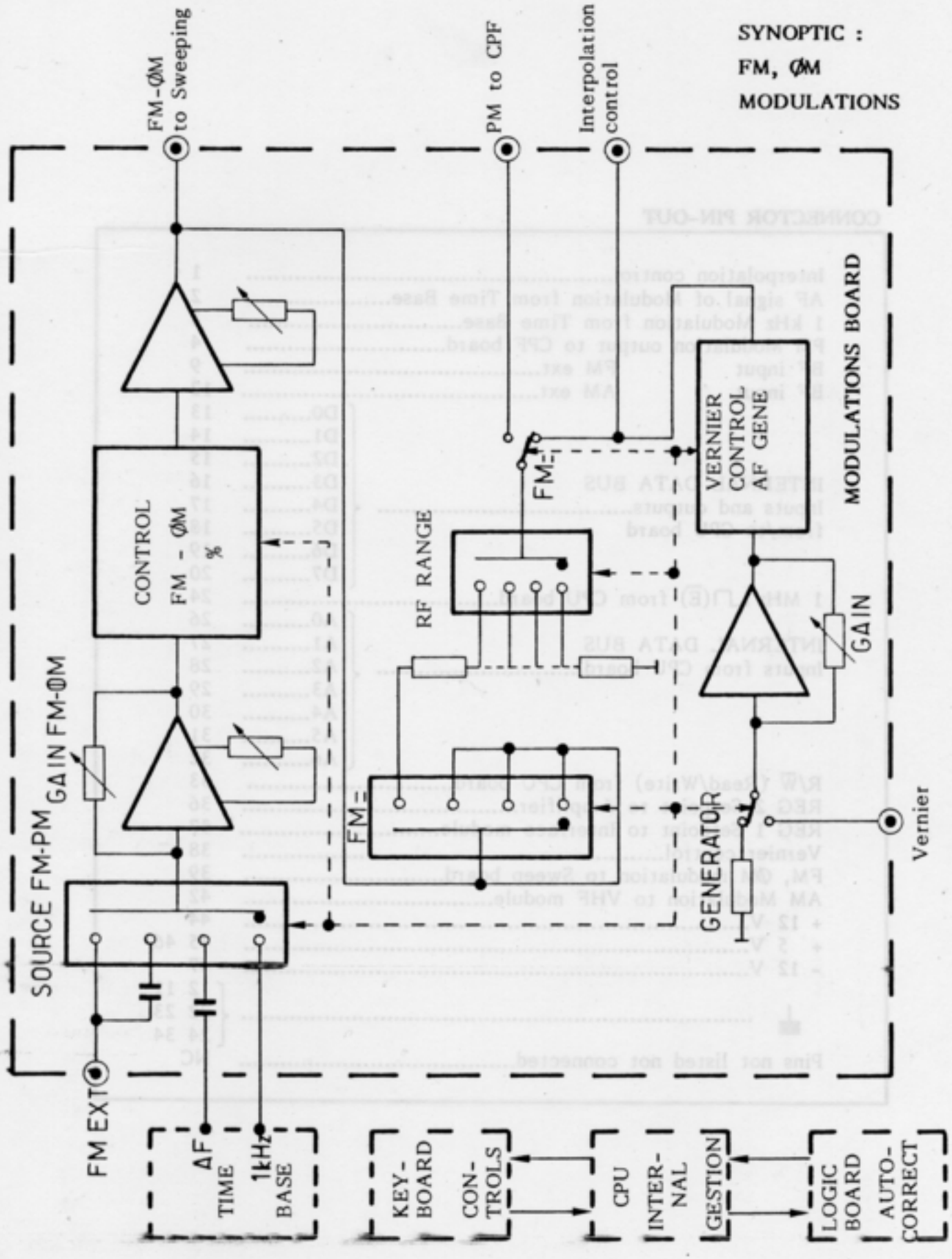
The 1 kHz internal AM or AF, or external AC/DC modulation source is selected by 4053 circuits SN20 and SN21, whose outputs are connected to LF356 transconductance amplifier SN22 which features gain adjustment P5. It drives AD7533 digital/analog converter SN17. The rate of modulation is applied to SN17, associated with LF356 amplifier SN23 on which a continuous shift of 2.5 V is performed using R38, R37 and P6. The modulating signal is output to the AM modulator of the VHF module, and to the input of the DAC for control of the Regulator 1 level reference recommended value.

FM, ØM MODULATION

The FM source, either internal at 1 kHz or AF, or external via direct AC or DC coupling, is selected by 4053 circuits SN5 and SN6. The output is connected to LF356 amplifier SN8 featuring DC component adjustment (P1) and FM gain adjustment (P2).
The signal then drives AD7533 digital/analog converter SN9, to which is applied the rate of FM drift. The signal is then transmitted across LF356 amplifier SN10, which features DC component adjustment P3, to the sweep board of the 20-25 MHz module, and to the 32-58 MHz oscillator of the phase comparator board for continuous PM and the interpolator for continuous FM.
In frequency modulation with DC coupling, the signal, after division in function of the RF range performed by 4053 3-into-2 divider SN6, is directed towards the interpolation oscillator. The selection of the various FM ranges is made on the interpolation board.
In case of phase modulation with DC coupling, the signal is delivered to the frequency phase comparator board ; 4053 3-into-1 switch SN12 selects the interpolator for continuous FM on pin 12, or the 32-58 MHz oscillator of the CPF board on pin 13.


SYNOPTIC :
AM MODULATION
To VHF AM Modulating
To INTERFACE
To AMPLIFIER
SETPOINT REG 1
SETPOINT REG 2
- 12 V
2.5 V unkeying
AM CONTROL %
ADJUSTMENT LF LEVEL
AM SOURCE
MODULATIONS BOARD
LOGIQUE BOARD AUTO CORRECTION
MICROPROCESSOR INTERNAL GESTION
KEYBOARD CONTROLS
AM EXT
TIME BASE
AF
1kHz

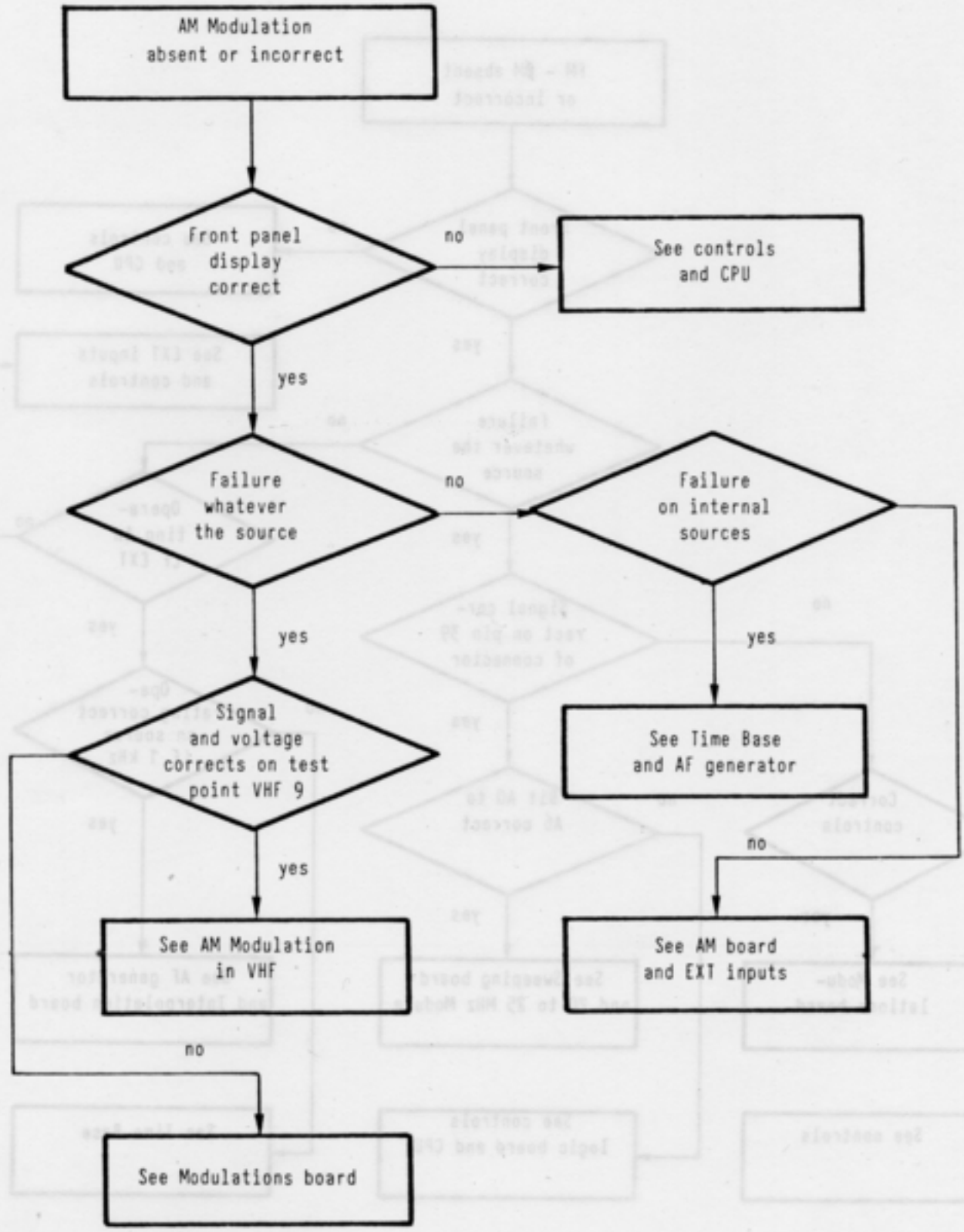
SYNOPTIC :
FM, ØM
MODULATIONS



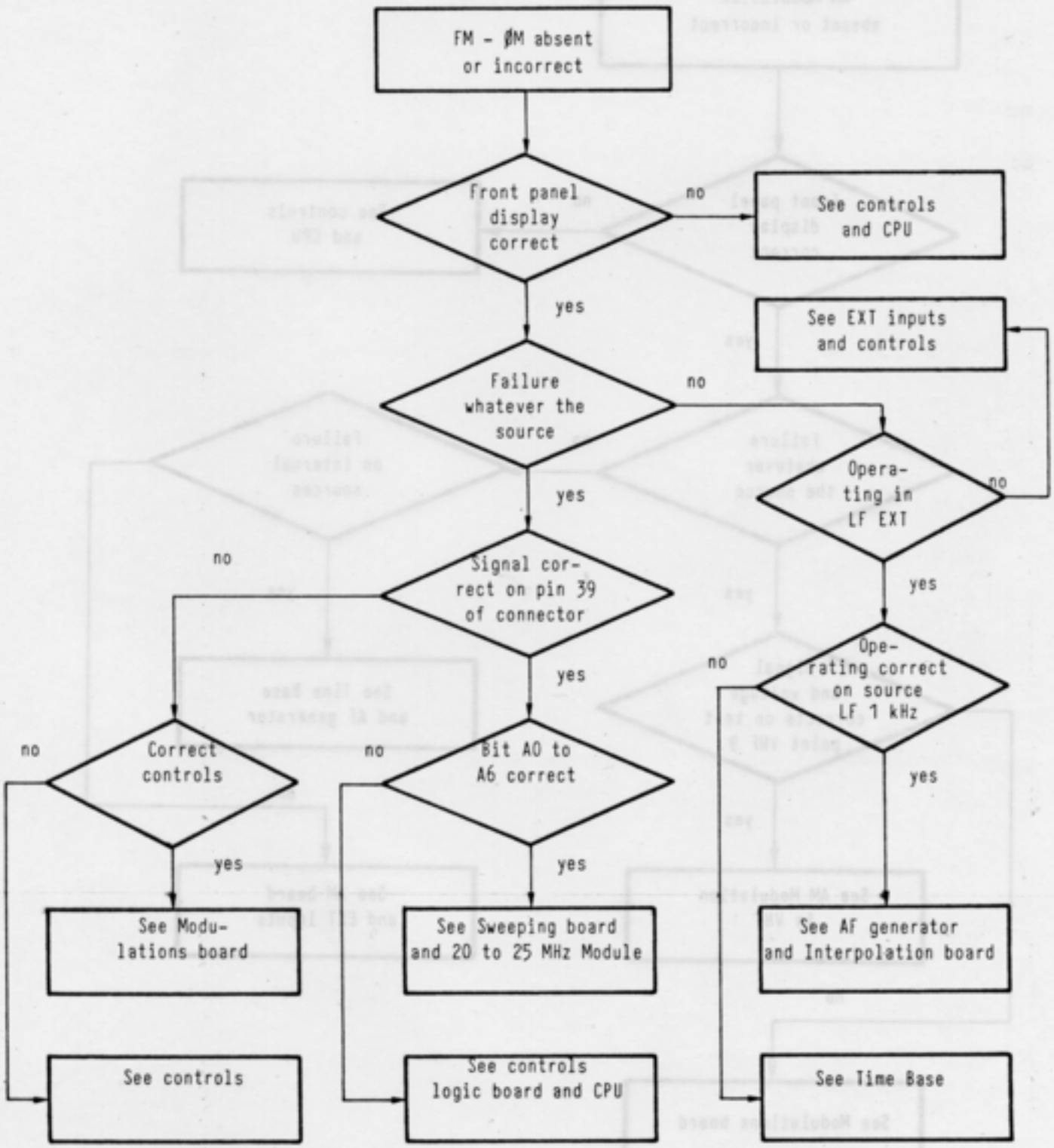
CONNECTOR PIN-OUT

Interpolation control		1
AF signal of Modulation from Time Base		2
1 kHz Modulation from Time Base		3
PM Modulation output to CPF board		4
BF input	FM ext	9
BF input	AM ext	12
INTERNAL DATA BUS Inputs and outputs from/to CPU board	D0	13
	D1	14
	D2	15
	D3	16
	D4	17
	D5	18
	D6	19
	D7	20
1 MHz ⊔⊓ ($\overline{E}$) from CPU board		24
INTERNAL DATA BUS Inputs from CPU board	A0	26
	A1	27
	A2	28
	A3	29
	A4	30
	A5	31
	A6	32
R/$\overline{W}$ (Read/Write) from CPU board		33
REG 2 Setpoint to Amplifier		36
REG 1 Setpoint to Interface module		37
Vernier control		38
FM, ØM modulation to Sweep board		39
AM Modulation to VHF module		42
+ 12 V		44
+ 5 V		45 46
- 12 V		47
⏚		2 11 22 23 24 34
Pins not listed not connected		NC

AM MODULATION



FM - ØM MODULATIONS



BOARD ADJUSTMENT

Equipment required

- 1 multimeter,
- 1 LF generator.

1) Check of Regulator 2

Set multimeter to DC operation on lug 36 of the connector.
a) in direct range
   Set + 10.9 dBm and read + 3 V.
   Set + 0.1 dBm and read + 1.9 V.
b) in doubled range
   Set 13 dBm and read 3.5 V.
c) For Fo < 1 MHz and whatever level set, read + 5 V.

2) Check of AM Modulation

Set multimeter to DC operation and connect to lug 42 of the board connector or the Test 9 connector on the VHF module.
Adjust potentiometer P6 to read 2.5 V.
Connect the multimeter in AC operation and position the 7200 in AM modulation with internal LF of 1 kHz. Adjust P5 to result in 1.77V RMS with 100% AM.
Check that at 80% there is read approximately 1.42 V RMS, and 0.89 V RMS at 50% AM.
Validate the AF generator at 1 kHz, with the 7200 in AM, AF mode and check that for 100% modulation, there results a value of 1.7 V RMS.
Validate external AM and inject an LF signal of 1 kHz on the front connector of the 7200, level 1 V RMS and check that for 100% modulation there, results a value of 1.77 V RMS.
Set the multimeter to DC, make a special 65, and read + 5 V.

3) Check of Regulator 1

Position the multimeter in DC operation on lug 37 of the connector.
In direct range, set + 10.9 dBm and read - 3.9 V RMS.
In direct range, set + 0.1 dBm and read - 1.1 V RMS.
In doubled range, set + 13 dBm and read - 5 V.

4) Check of FM, ØM functions

- Position the multimeter in DC operation on lug 39 of the connector.
- Set 0 kHz deviation and adjust P3 to suppress the DC component.
- Set 300 kHz deviation and adjust P1 to suppress the DC component.
- Position the multimeter in AC operation and set FM mode with 1 kHz internal, and adjust P2 to result in 3 V RMS in FM at 300 kHz fromΔF.
- Check that at 100 kHz fromΔF, there results 1 V RMS, and at 50 kHz fromΔF, there results 0.5 V RMS.
- Check that by setting 300 kHz fromΔF, there results 3 V RMS.
- Validate external FM and inject an LF signal of 1 kHz on the front connector of the 7200, level 1 V RMS and check that by setting 300 kHz fromΔF, there results 3 V RMS.

- Inject a frequency of 20 Hz with level of 1 V RMS on the external DC PM connector. Set ØM, 300 degrees.
- Position the multimeter in AC operation on lug 4 of the connector. There should result the following values for :

F = 100 MHz	3 V RMS
F = 200 MHz	1.5 V RMS
F = 400 MHz	0.65 V RMS
F = 800 MHz	0.3 V RMS

5) Check of vernier control and AF generator

Position the multimeter in DC operation on lug 1 of SN15. Validate the vernier.
Adjust P4 to read - 3.41 V.

FRONT PANEL ASSEMBLY

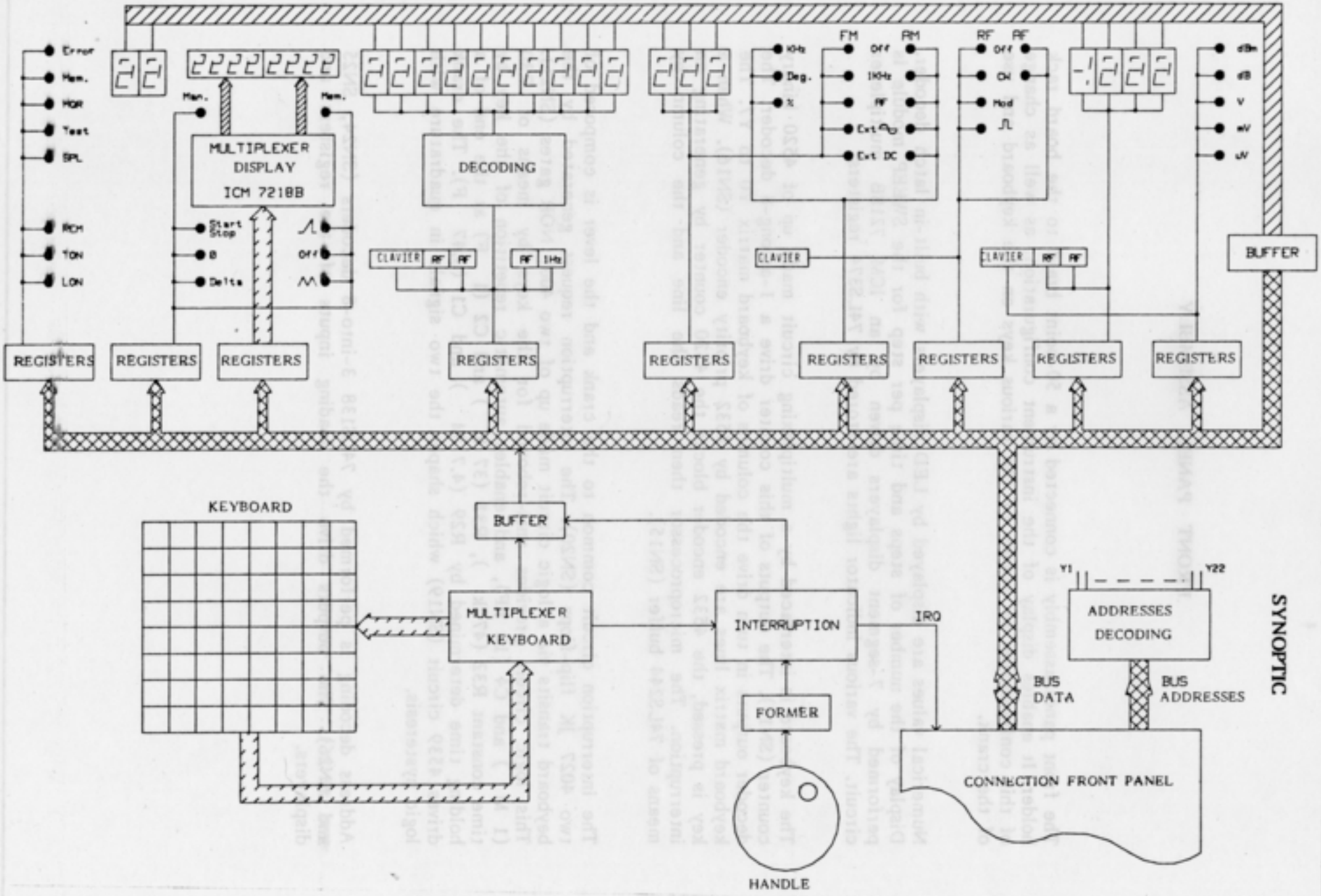
The front panel assembly is connected by a 50-point braid to the board rack holder. It enables display of the instrument configuration, as well as change of this configuration by means of the various keys on the keyboard and use of the crank.

Numerical values are displayed by LED displayers with built-in latch decoder. Display of the number of steps and time per step for the SWEEP module is performed by 7-segment displayers driven by an ICM 7218B multiplexer circuit. The various indicator lights are stored by 74LS374 registers.

The keyboard is interfaced by a multiplexing circuit made up of 4520 binary counter (SN17). The outputs of this counter drive a 1-among-8 decoder. The decoder outputs in turn drive the columns of keyboard matrix Y0 to Y7. The keyboard matrix lines are encoded by 4532 priority encoder (SN16). When a key is pressed, the 4532 encoder blocks the 4520 counter by generating an interruption. The microprocessor then reads the line and the column by means of 74LS244 buffer (SN15).

The interruption circuit common to the crank and the lever is composed of two 4027 JK flip-flops (SN20). The interruption request generated by the beyboard transits via a logic circuit made up of two 4001 NOR gates (SN21). This logic circuit provides anti-rebound for the keys by means of R30 (1 M) and C4 (10 nF), and enables automatic repetition of the key by time constant R32 (47 k), R31 (37 k) and C2 (1 F) at the end of a holding time determined by R29 (4.7 M) and C1 (0.47 F). The crank drives 4539 circuit (SN19) which shapes the two signals in quadrature with logic hysteresis.

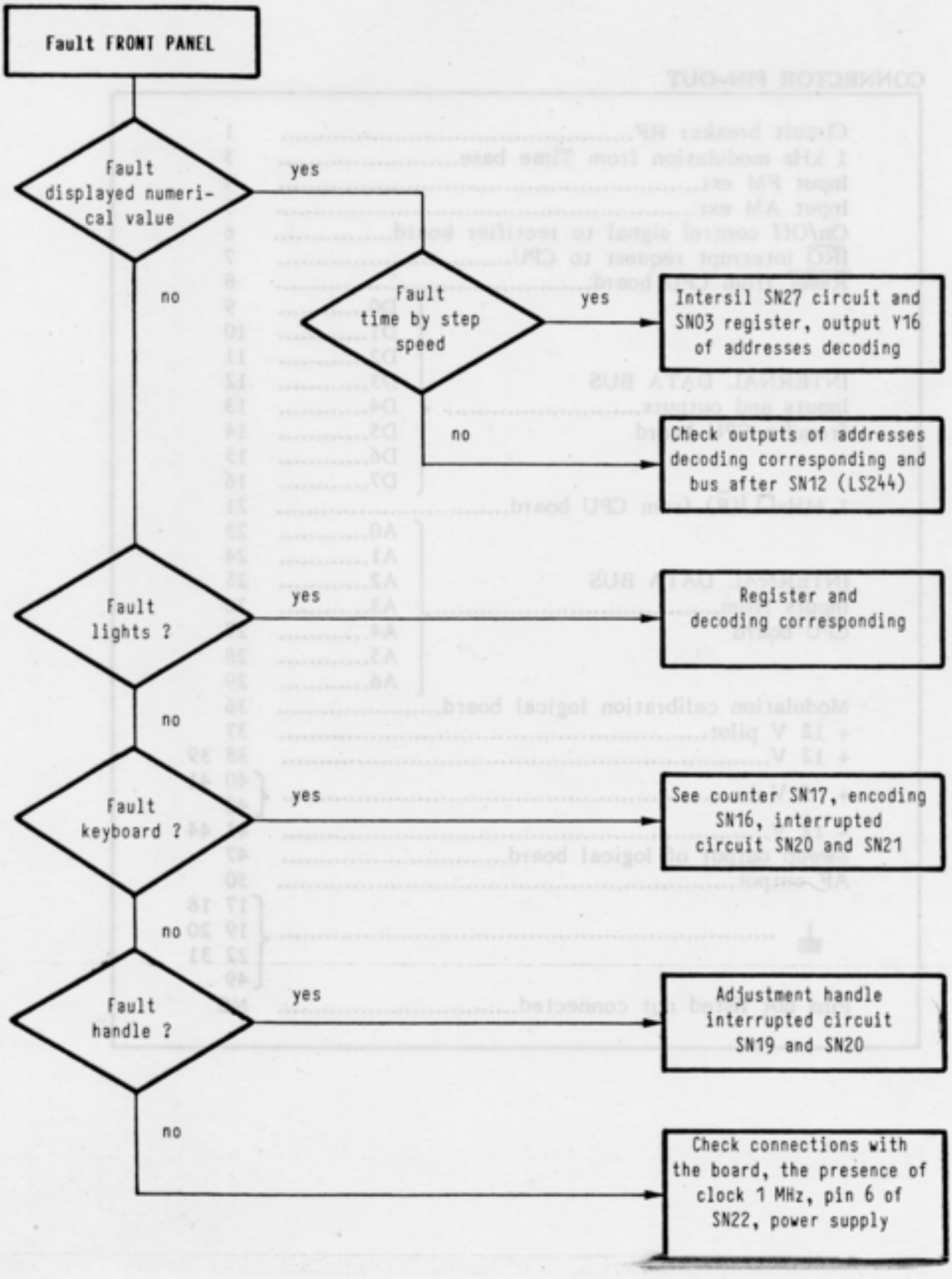
Address decoding is performed by 74LS138 3-into-8 decoders (SN24, SN25 and SN26). The outputs drive the loading inputs of the registers and displayers.


Error
Mem.
MOR
Test
SPL
RCH
TON
LON
MULTIPLEXER
DISPLAY
ICM 7218B
Start
Stop
Delta
DECODING
CLAVIER
RF
AF
AF
1Hz
kHz
Deg.
%
FM
AM
Off
1KHz
Ext DC
Ext AC
Mod
dBm
dB
V
mV
uV
BUFFER
REGISTERS
KEYBOARD
MULTIPLEXER
KEYBOARD
INTERRUPTION
IRQ
FORMER
HANDLE
Y1
Y22
ADDRESSES
DECODING
BUS
DATA
BUS
ADDRESSES
CONNECTION FRONT PANEL
SYNOPTIC

CONNECTOR PIN-OUT

Circuit breaker RF		1
1 kHz modulation from Time base		3
Input FM ext		4
Input AM ext		5
On/Off control signal to rectifier board		6
$\overline{IRQ}$ interrupt request to CPU		7
Reset from CPU board		8
INTERNAL DATA BUS Inputs and outputs from/to CPU board	D0	9
	D1	10
	D2	11
	D3	12
	D4	13
	D5	14
	D6	15
	D7	16
1 MHz⊓⊔($\overline{E}$) from CPU board		21
INTERNAL DATA BUS Inputs from CPU board	A0	23
	A1	24
	A2	25
	A3	26
	A4	27
	A5	28
	A6	29
Modulation calibration logical board		36
+ 12 V pilot		37
+ 12 V		38 39
+ 5 V		40 41 42
- 12 V		43 44
Sweep output of logical board		47
AF output		50
⏚		17 18 19 20 22 31 49
Pins not listed not connected		NC

TROUBLESHOOTING CHART

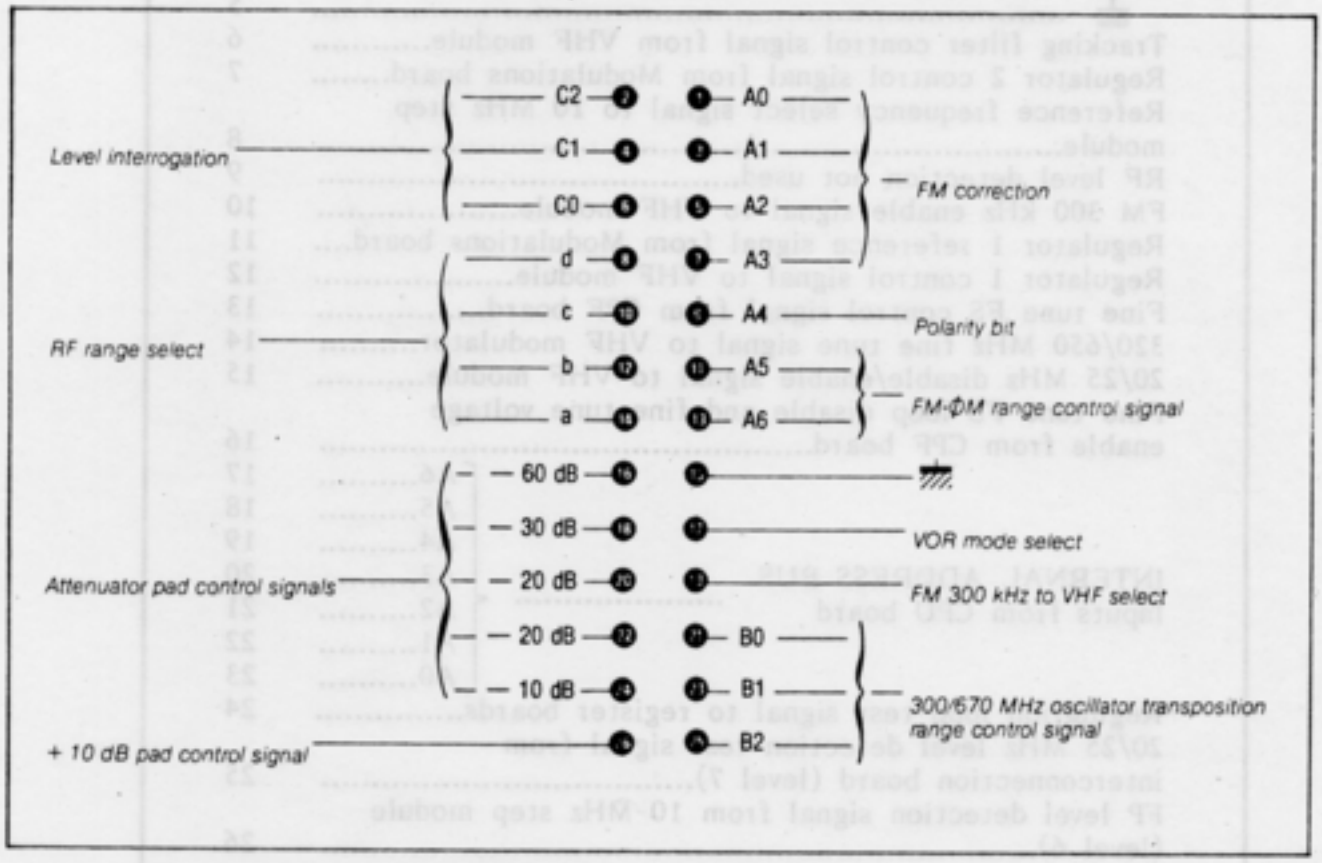


INTERFACE MODULE

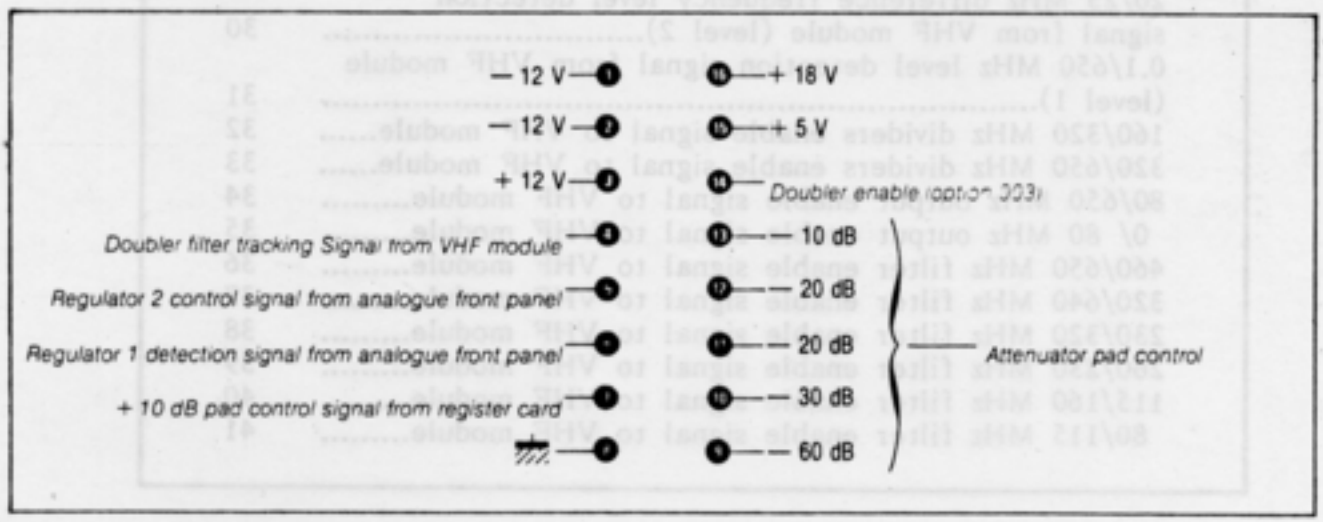
MAIN CONNECTOR PIN-OUT

- 12 V	1
+ 5 V	2
+ 12 V	3
+ 18 V	4
⏚	5
Tracking filter control signal from VHF module	6
Regulator 2 control signal from Modulations board	7
Reference frequency select signal to 10 MHz step module	8
RF level detection not used	9
FM 300 kHz enable signal to VHF module	10
Regulator 1 reference signal from Modulations board	11
Regulator 1 control signal to VHF module	12
Fine tune FS control signal from CPF board	13
320/650 MHz fine tune signal to VHF modulator	14
20/25 MHz disable/enable signal to VHF module	15
Fine tune FS loop disable and fine tune voltage enable from CPF board	16
INTERNAL ADDRESS BUS Inputs from CPU board — A6	17
A5	18
A4	19
A3	20
A2	21
A1	22
A0	23
Régulation loop test signal to register boards	24
20/25 MHz level detection test signal from interconnection board (level 7)	25
FP level detection signal from 10 MHz step module (level 6)	26
400 MHz level detection signal from 10 MHz step module (level 5)	27
FP/40 level detection signal from 10 MHz step module (level 4)	28
FS/40 level detection signal from VHF module (level 3)	29
20/25 MHz difference frequency level detection signal from VHF module (level 2)	30
0.1/650 MHz level detection signal from VHF module (level 1)	31
160/320 MHz dividers enable signal to VHF module	32
320/650 MHz dividers enable signal to VHF module	33
80/650 MHz output enable signal to VHF module	34
0/ 80 MHz output enable signal to VHF module	35
460/650 MHz filter enable signal to VHF module	36
320/640 MHz filter enable signal to VHF module	37
230/320 MHz filter enable signal to VHF module	38
260/230 MHz filter enable signal to VHF module	39
115/160 MHz filter enable signal to VHF module	40
80/115 MHz filter enable signal to VHF module	41

INTERFACE/REGISTER CONNECTOR



AMPLIFIER COMMAND/INTERFACE CONNECTOR



BOARD ACCESS

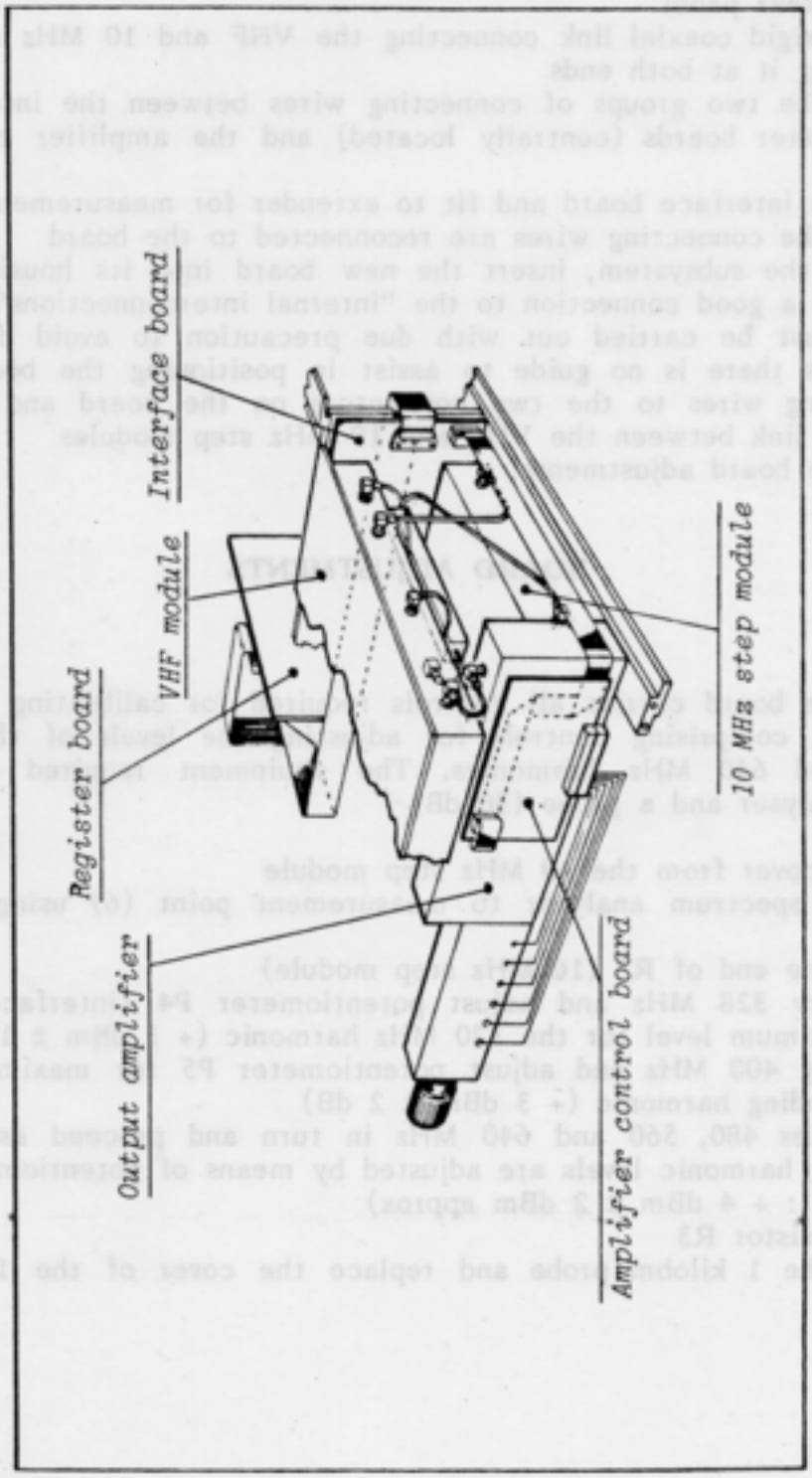
The interface board is accessible from the rear of the generator

a) Remove the rear panel
b) Remove the rigid coaxial link connecting the VHF and 10 MHz step modules by unscrewing it at both ends
c) Disconnect the two groups of connecting wires between the interface board and the register boards (centrally located) and the amplifier control board (at bottom)
d) Withdraw the interface board and fit to extender for measurements and tests. Check that the connecting wires are reconnected to the board
e) If replacing the subsystem, insert the new board into its housing, checking that there is a good connection to the "internal interconnections" board. This operation must be carried out with due precaution to avoid damaging the connector, as there is no guide to assist in positioning the board. Connect the connecting wires to the two connectors on the board and replace the rigid coaxial link between the VHF and 10 MHz step modules
f) Carry out the board adjustments

BOARD ADJUSTMENTS

The interface board carries all controls required for calibrating the 10 MHz step module, comprising controls for adjusting the levels of the 320, 400, 480, 560 and 640 MHz harmonics. The equipment required comprises a spectrum analyser and a probe (30 dB)

a) Remove the cover from the 10 MHz step module
b) Connect the spectrum analyser to measurement point (6) using the 30 dB probe
c) Disconnect one end of R3 (10 MHz step module)
d) Set frequency 328 MHz and adjust potentiometer P4 (interface board) to obtain a maximum level for the 320 MHz harmonic (+ 1 dBm ± 1 dB)
e) Set frequency 400 MHz and adjust potentiometer P5 for maximum level of the corresponding harmonic (+ 3 dBm ± 2 dB)
f) Set frequencies 480, 560 and 640 MHz in turn and proceed as above. The corresponding harmonic levels are adjusted by means of potentiometers P3, P2 and P1 (level : + 4 dBm ± 2 dBm approx)
g) Reconnect resistor R3
h) Disconnect the 1 kilohm probe and replace the cover of the 10 MHz step module


Interface board
VHF module
Register board
Output amplifier
10 MHz step module
Amplifier control board

20 - 25 MHz MODULE - SWEEP BOARD

This module comprises the 80/100 MHz oscillator and the associated divide by four and phase lock circuits. With the **SWEEP** board, the oscillator is rapidly locking for the sweeping function or SPL 29 function.
The tuned circuit of the 80/100 MHz Clapp oscillator comprises coil T2, capacitors C2 and C3, varicap diodes D1 to D8 and trimming capacitor C5. The output frequency of this oscillator is divided by four by means of two J-K bistables (integrated circuit SN1) to obtain the 20/25 MHz signal which is input to the **PHASE-FREQUENCY COMPARATOR** subsystem and VHF module.

The 80/100 MHz oscillator is locked onto pulses output by the phase-frequency comparator of the counter subsystem. These pulses are integrated by an active threepole filter (integrated circuit SN2) followed by an RC circuit comprising resistor R40 and capacitors C30-C38 on the dynamic channel and by means of a current pull-up circuit (transistors Q11 to Q14) on the static channel. An accelerator circuit comprising transistors Q15 to Q18 and integrator R56-C39 senses the width of output pulses from the counter subsystem and is used to reduce the time constant of the phase-lock circuit by a factor of 100 under transient conditions. The sweeping process described above is that used in case of the equipment is operated purely as a **GENERATOR.**

When the equipment is used for frequency sweeping or in SPL 29 function, the sweeping method for the 80 - 100 MHz oscillator is different.

First of all, the 20 - 25 MHz **SWEEPING** board performs this new high-speed slaving function, as well as selection of ØM and FM modulation (3 - 30 and 300 kHz ranges), and shaping of modulating signal level in function of the RF range used, plus inversion of the LF signal when the 80 - 100 MHz oscillator operates in inverse spectrum with respect to the output frequency.

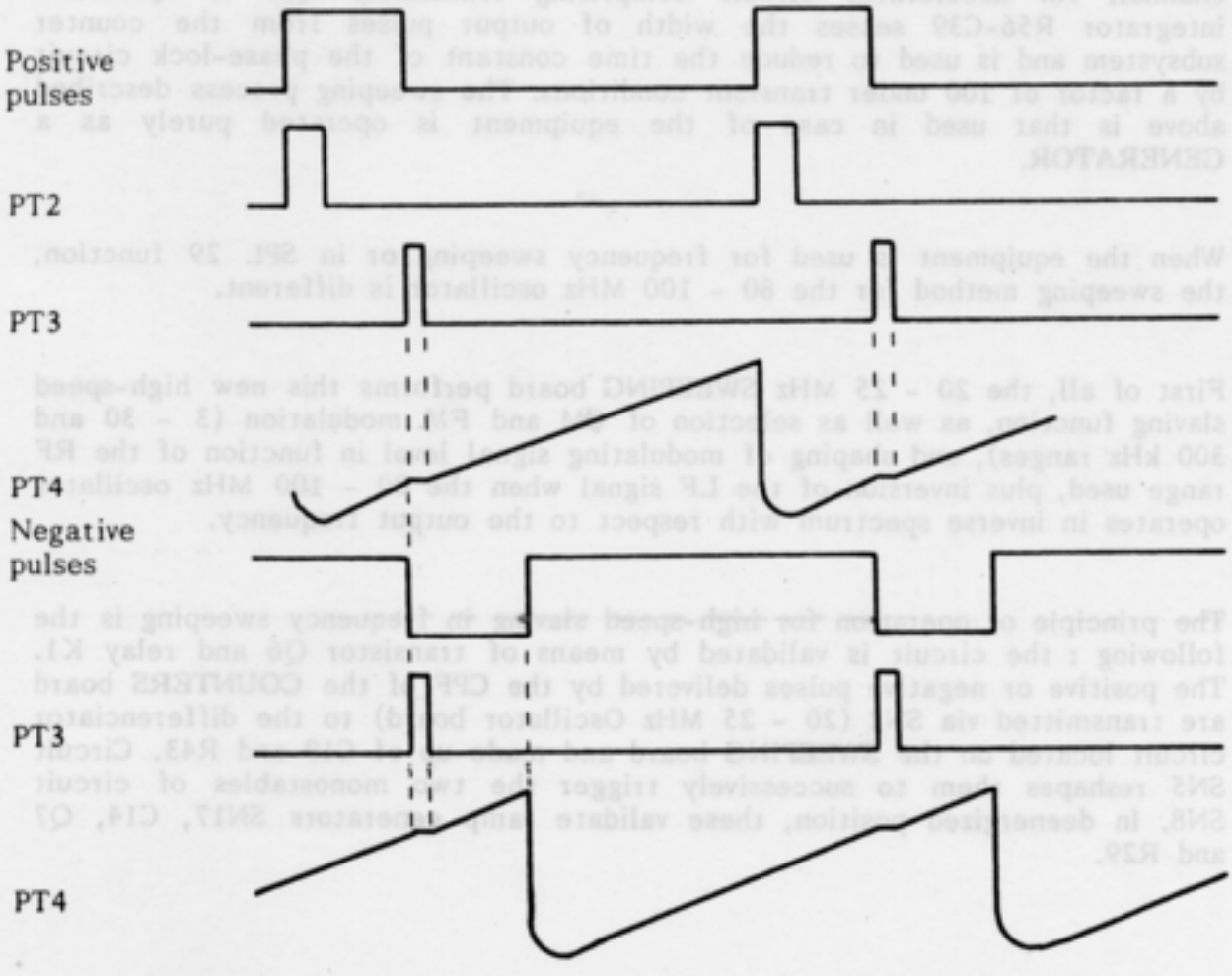
The principle of operation for high-speed slaving in frequency sweeping is the following : the circuit is validated by means of transistor Q6 and relay K1. The positive or negative pulses delivered by the CPF of the **COUNTERS** board are transmitted via SN2 (20 - 25 MHz Oscillator board) to the differenciator circuit located on the **SWEEPING** board and made up of C19 and R43. Circuit SN5 reshapes them to successively trigger the two monostables of circuit SN8. In deenergized position, these validate ramp generators SN17, C14, Q7 and R29.

If there are positive pulses output from the CPF (Counters board), the leading edge triggers a reset of the ramp ; C14 is short-circuited by SN9 by means of the 70 μs control pulse at PT2. The trailing edge triggers the second monostable which delivers a pulse with a duration of approximately 10 μs. This latter stops the loading of C14, and transfers at the same time the corresponding potential on the oscillator control. It may be seen that pulse width determines the oscillator control voltage, and pulse polarity determines its variation direction for frequency acquisition.

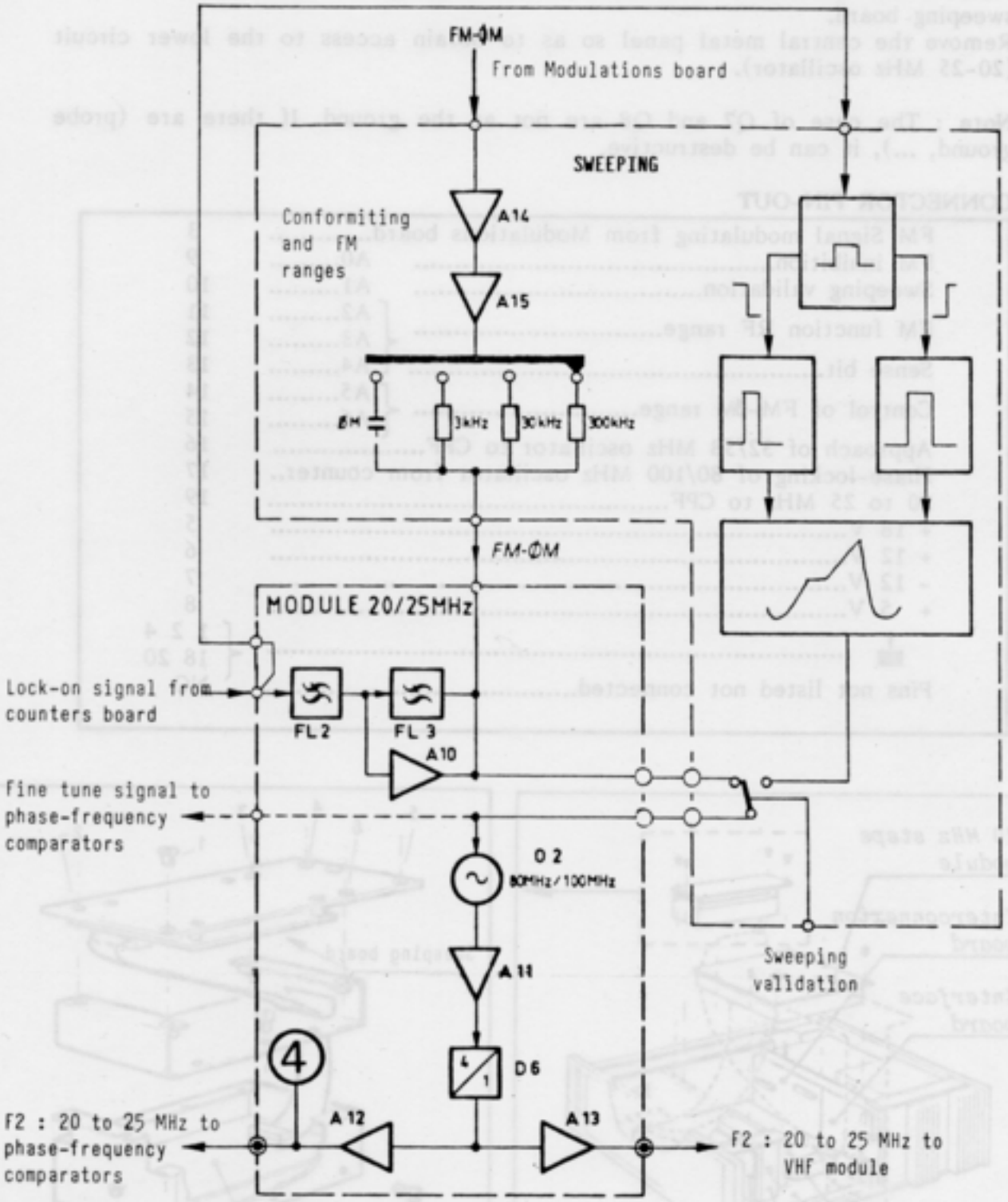
The LF signal is inverted by circuits SN4 and SN6. This latter also selects LF level in function of the RF range. It is rendered inoperative by the "Inhib FM" bit.

The various FM ranges and the ØM function are obtained in circuits SN2 and SN3 associated with R9, R10, R11, C5 and C6.

CHRONOGRAM



SYNOPTIC


FM-ΦM
From Modulations board
SWEEPING
Conformiting and FM ranges
A14
A15
BM
3kHz
30kHz
300kHz
FM-ΦM
MODULE 20/25MHz
Lock-on signal from counters board
FL2
FL 3
A10
Fine tune signal to phase-frequency comparators
O 2
80MHz/100MHz
A11
D6
4
1
A12
A13
F2 : 20 to 25 MHz to phase-frequency comparators
F2 : 20 to 25 MHz to VHF module
Sweeping validation

MODULE TESTS

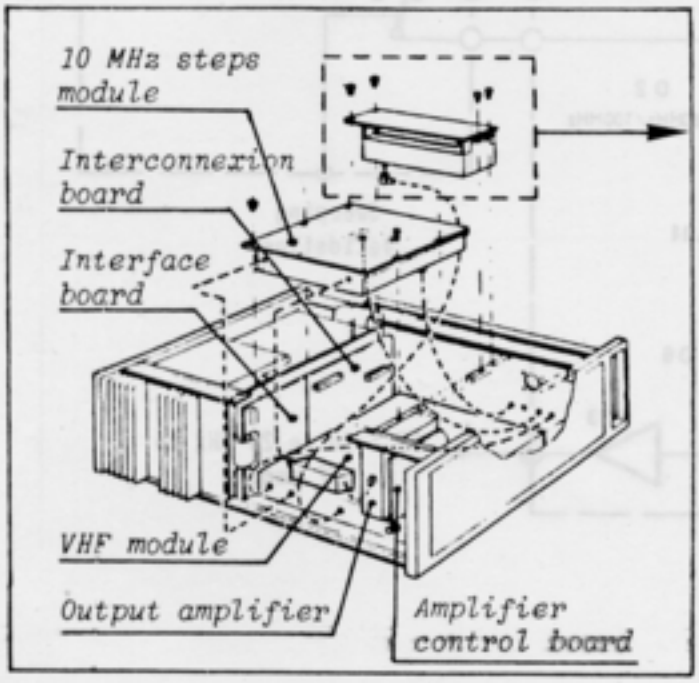
Preparation

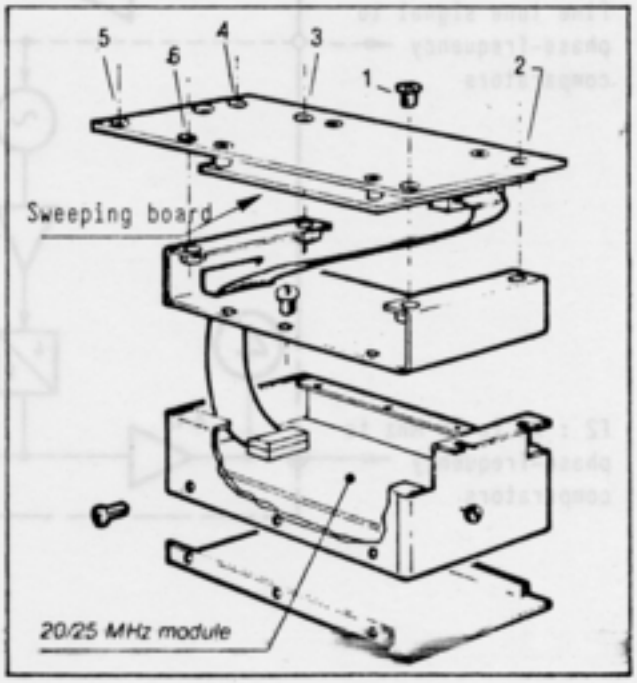
- Remove the generator bottom panel. The 20-25 MHz module (reference 027146) is mounted adjacent the 10 MHz step module.
- Remove the six screws indicated on the diagram to obtain access to the sweeping board.
- Remove the central metal panel so as to obtain access to the lower circuit (20-25 MHz oscillator).

Nota : The case of Q7 and Q8 are not at the ground. If there are (probe ground, ...), it can be destructive.

CONNECTOR PIN-OUT

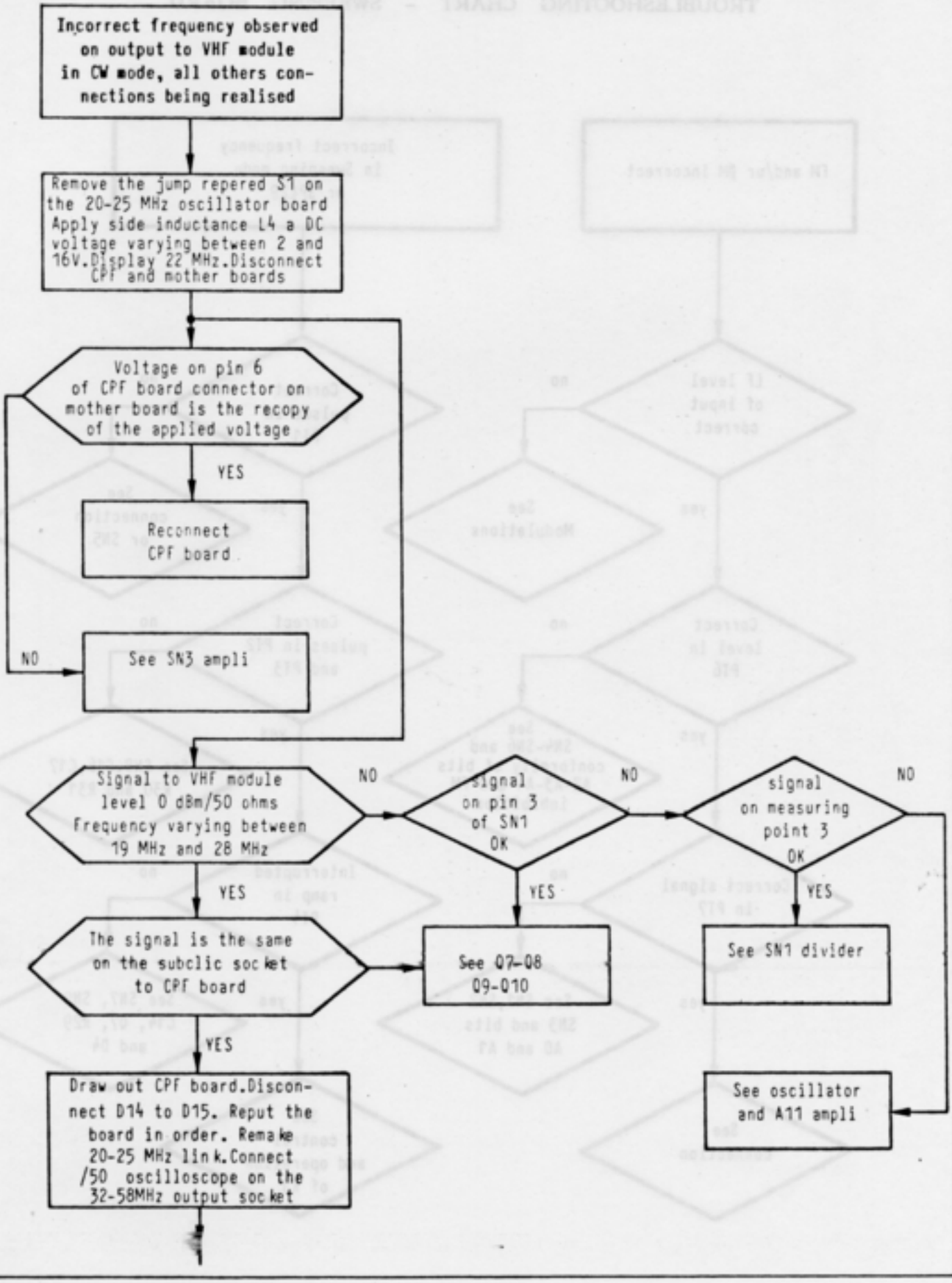
FM Signal modulating from Modulations board		3
FM inhibition	A0	9
Sweeping validation	A1	10
FM function RF range	A2	11
	A3	12
Sense bit	A4	13
Control of FM-ØM range	A5	14
	A6	15
Approach of 32/58 MHz oscillator to CPF		16
Phase-locking of 80/100 MHz oscillator from counter		17
20 to 25 MHz to CPF		19
+ 18 V		5
+ 12 V		6
- 12 V		7
+ 5 V		8
⏚		1 2 4 18 20
Pins not listed not connected		NC

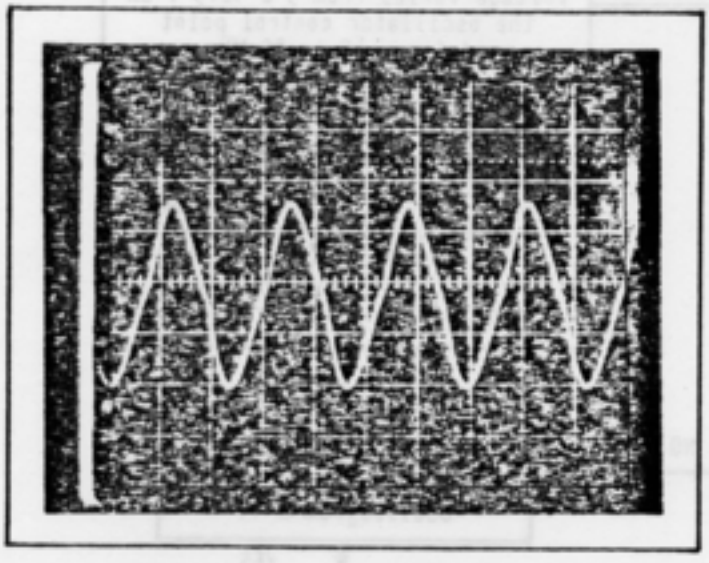




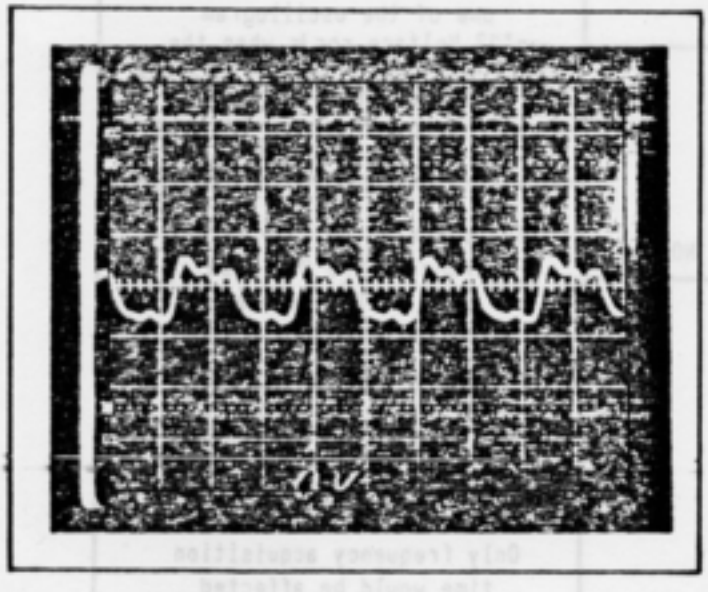
TROUBLESHOOTING CHART - SWEEPING BOARD

TROUBLESHOOTING CHART

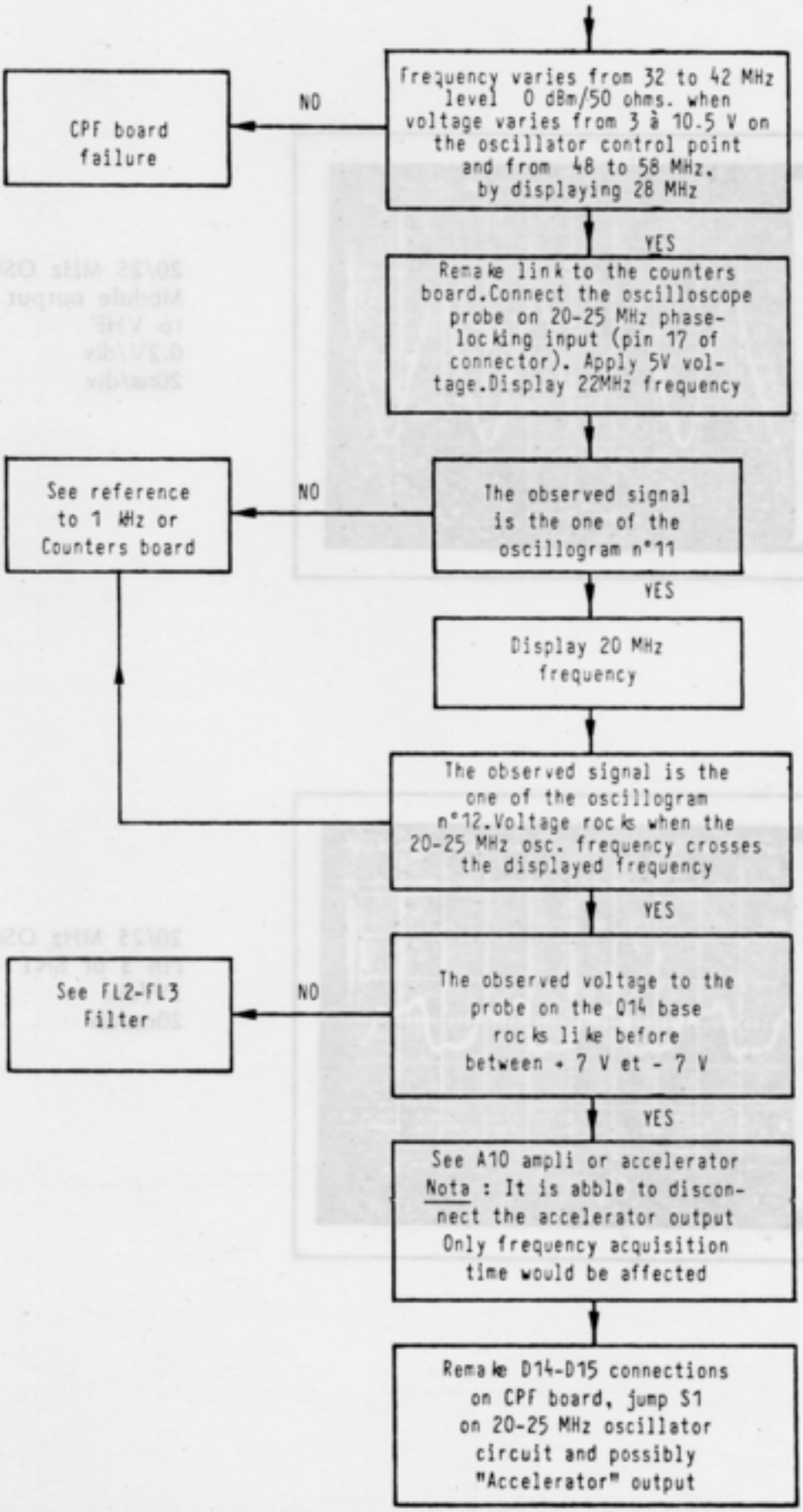


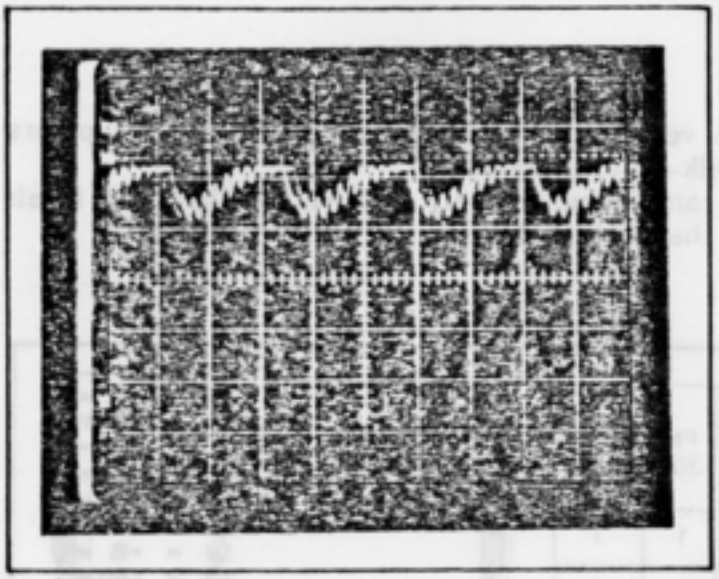


20/25 MHz OSC.
Module output
to VHF
0.2V/div
20ns/div

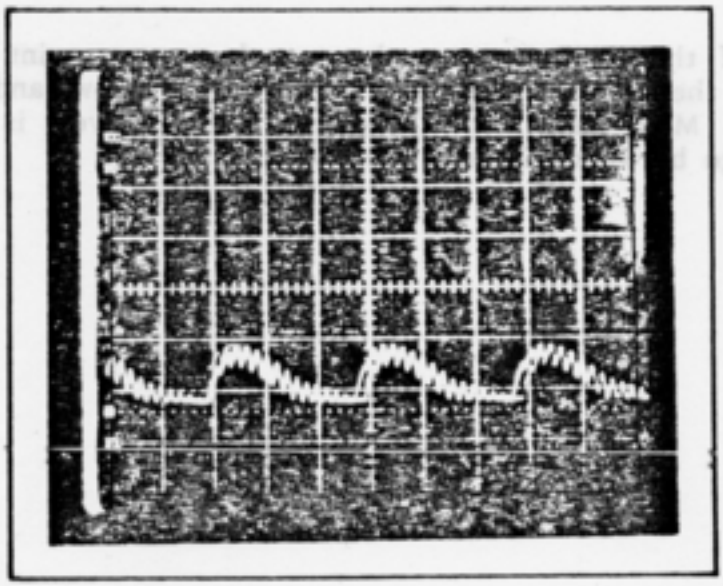


20/25 MHz OSC.
Pin 3 of SN1
1V/div
20ns/div


Frequency varies from 32 to 42 MHz level 0 dBm/50 ohms. when voltage varies from 3 à 10.5 V on the oscillator control point and from 48 to 58 MHz. by displaying 28 MHz
NO
CPF board failure
YES
Remake link to the counters board.Connect the oscilloscope probe on 20-25 MHz phase-locking input (pin 17 of connector). Apply 5V voltage.Display 22MHz frequency
The observed signal is the one of the oscillogram n°11
NO
See reference to 1 MHz or Counters board
YES
Display 20 MHz frequency
The observed signal is the one of the oscillogram n°12.Voltage rocks when the 20-25 MHz osc. frequency crosses the displayed frequency
YES
The observed voltage to the probe on the Q14 base rocks like before between + 7 V et - 7 V
NO
See FL2-FL3 Filter
YES
See A10 ampli or accelerator
Nota : It is abble to disconnect the accelerator output Only frequency acquisition time would be affected
Remake D14-D15 connections on CPF board, jump S1 on 20-25 MHz oscillator circuit and possibly "Accelerator" output



Oscillogram n°11
Phase locking input
pin 17 of connector
20/25 MHz
5V/div
5ms/div



Oscillogram n°12
Phase locking input
pin 17 of connector
20/25 MHz
5V/div
5ms/div

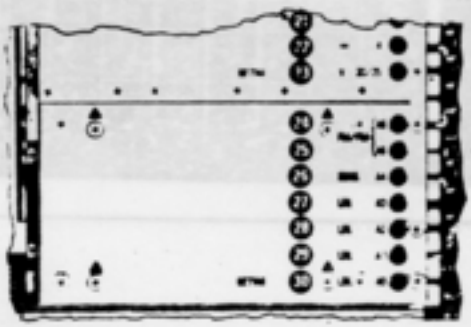
DEVIATION RANGE CONTROLS

DEVIATION RANGES

The FM deviation ranges are verified by testing the levels at test points on the top panel repered with silk-screened symbols
Select the FM-ØM deviation ranges successively and verify that the levels at points 24 and 25 are as per the table below :

Range / Mark	ØM	FM 3K	FM 30K	FM 300K
24	0	0	1	1
25	0	1	1	0

«0» = 0 V ; «1» = ≃7,5 V.



OSCILLATOR ADVANCE

The direction of advance of the oscillator may be tested at test point 26 which is low (0 V) when the 1 MHz steps are 4 MHz or below and 0 (+ 7.5 V) for the 5 to 9 MHz steps (the 1 MHz steps displayed is in according to the direct range between 325 and 650 MHz).

MODULE ADJUSTMENTS

MODULE REPAIRED

Equipment required :
- Multimeter,
- Spectrum analyser,
- Panoramic spectrum analyser,
- Modulation meter,
- Oscilloscope

1) Level check

a) Short-circuit the base and emitter of Q1 to disable the oscillator

b) Set 605 MHz and check the voltages at the following points, which are marked on the electrical circuit diagram :

1 : - 2 V ± 0.2 V ; 2 : + 8.5 V ± 0.5 V ; 3 : + 3.75 V ± 0.1 V

c) Remove the short-circuit from transistor Q1

2) Oscillator calibration

Connect the multimeter to the bypass marked "U asservissement 20/25" accessible from beneath the instrument. Adjust capacitor C5 on the 20/25 MHz board to obtain a level of 10,3 V at the measurement point when the frequency set is 605 MHz. Set 600 MHz and check that the level is now not more than 3 ± 0.1 V

3) Signal-shaping circuit and 20-25 MHz output test

a) Connect the spectrum analyser to measurement point (2) using a 30 dB probe

b) Set 605 MHz and check that the signal level is + 6 ± 1 dBm

c) Connect the analyser to the module coaxial output. Balance winding T1 to obtain an output level of 0 ± 1 dBm at 600 MHz and 605 MHz

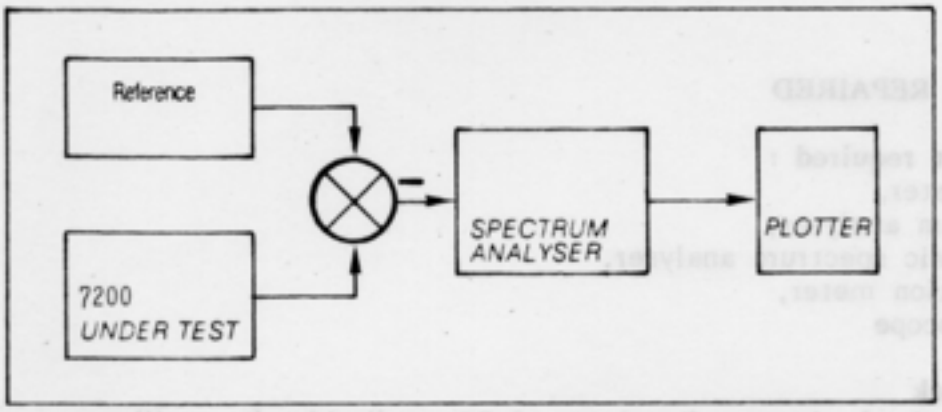
4) Lock-on circuit accelerator

a) Connect the oscilloscope to the collector of Q17 and check for the presence of negative-going pulses on selecting the 1 MHz step. Check for the presence of positive-going pulses at the collector of Q18

b) Connect the oscilloscope to the "Asservi 20/25" by-pass and set 602.5 MHz. Centre the oscilloscope (set to DC) and adjust P01 to cancel the AC component at 1 kHz so as to centre on the DC 0 point. Select 1 MHz step and check that the DC 0 is stabilised to within ± 100 mV

5) Oscillator noise

a) Measurement principle (module closed and in situ in instrument) :



b) Measure on the direct 320-650 MHz range at 340 and 345 MHz

c) Check that the noise level at 1 and 10 kHz of the carrier is below - 110 dB and - 140 dB, respectively

REMOVING AND REPLACING THE MODULE

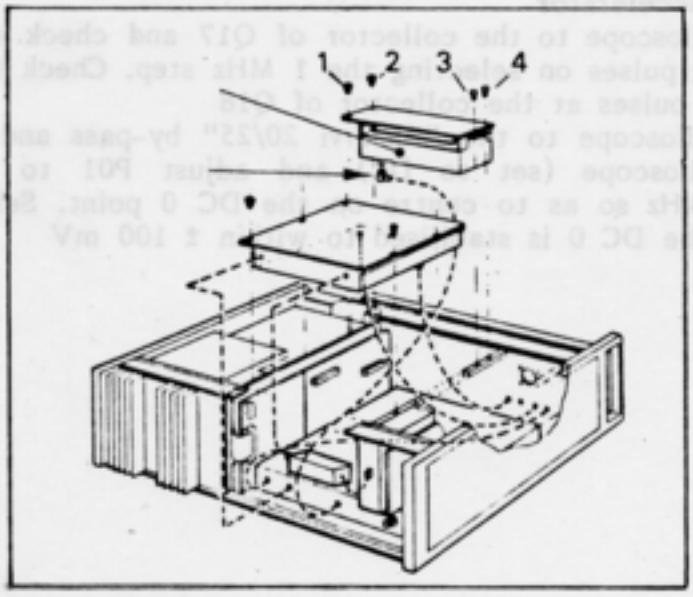
a) Remove the bottom panel from the instrument

b) The 20-25 MHz module (027146) is adjacent the 10 MHz step module

c) Remove the four retaining screws marked on the diagram to release the module from its housing. Pull out carefully as a coaxial connection is made to the opposite end of the module

d) Unscrew the end of the coaxial connection and remove the module

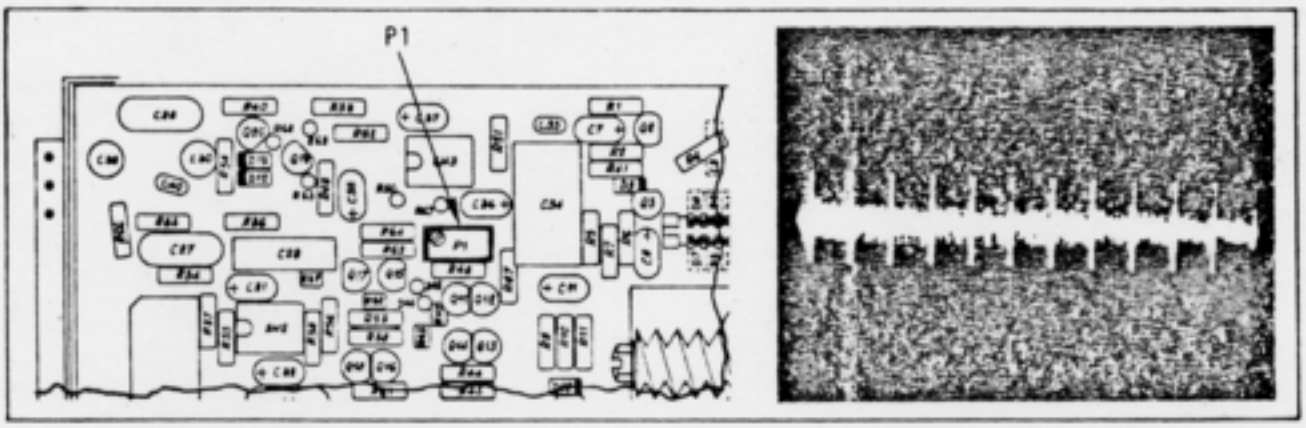
e) Replace the coaxial connection to the replacement module, place in the housing and attach to the instrument chassis



MODULE CALIBRATION
(module replaced or not)

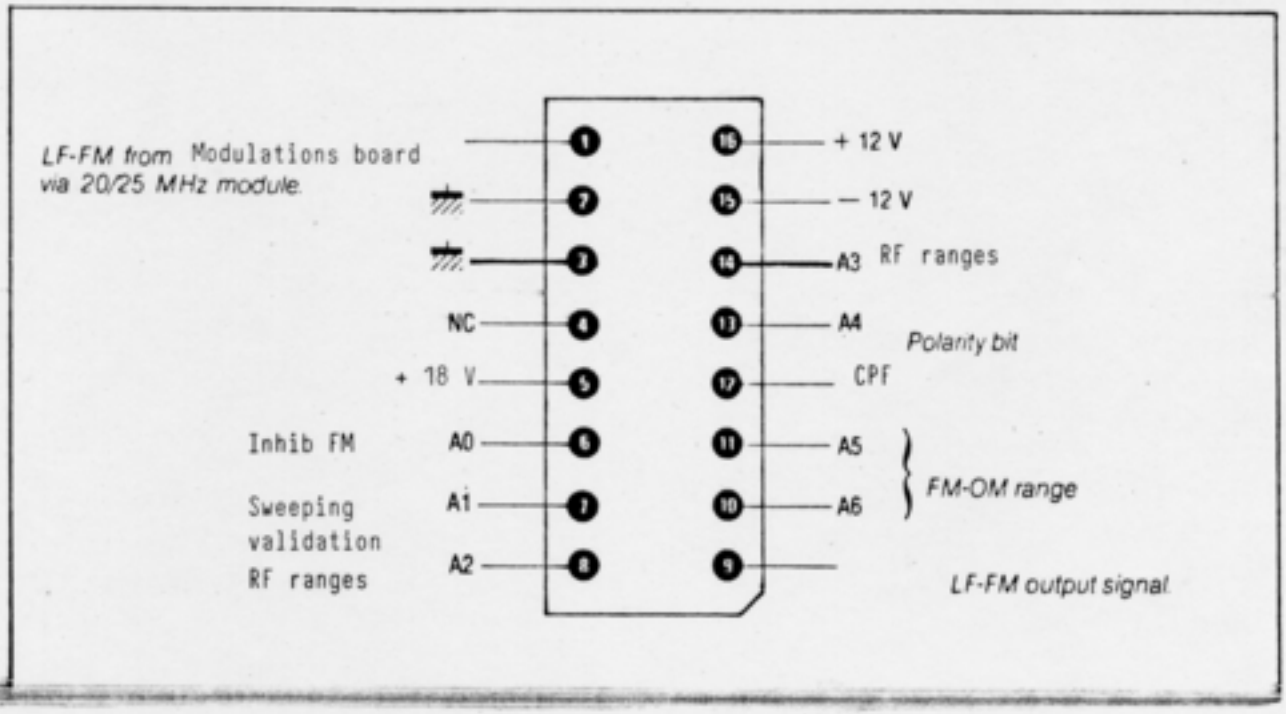
1 kHz residual

a) Open up the module a described in the section on "preparation" to obtain access to the adjustment potentiometer on the 20 - 25 MHz oscillator board
b) Set a frequency of 2,5 MHz
c) Connect oscilloscope to test point 23 on the bottom surface of the generator (marked 23 V 20/25)
d) Adjust potentiometer P1 to minimise the level of 1 kHz residual
e) Check that the frequency component levels are approximately 200 mVpeak from 10 to 15 MHz



CONNECTING WIRE BUNDLE SUPPORT MARKINGS

/20-25 MHz module interconnections



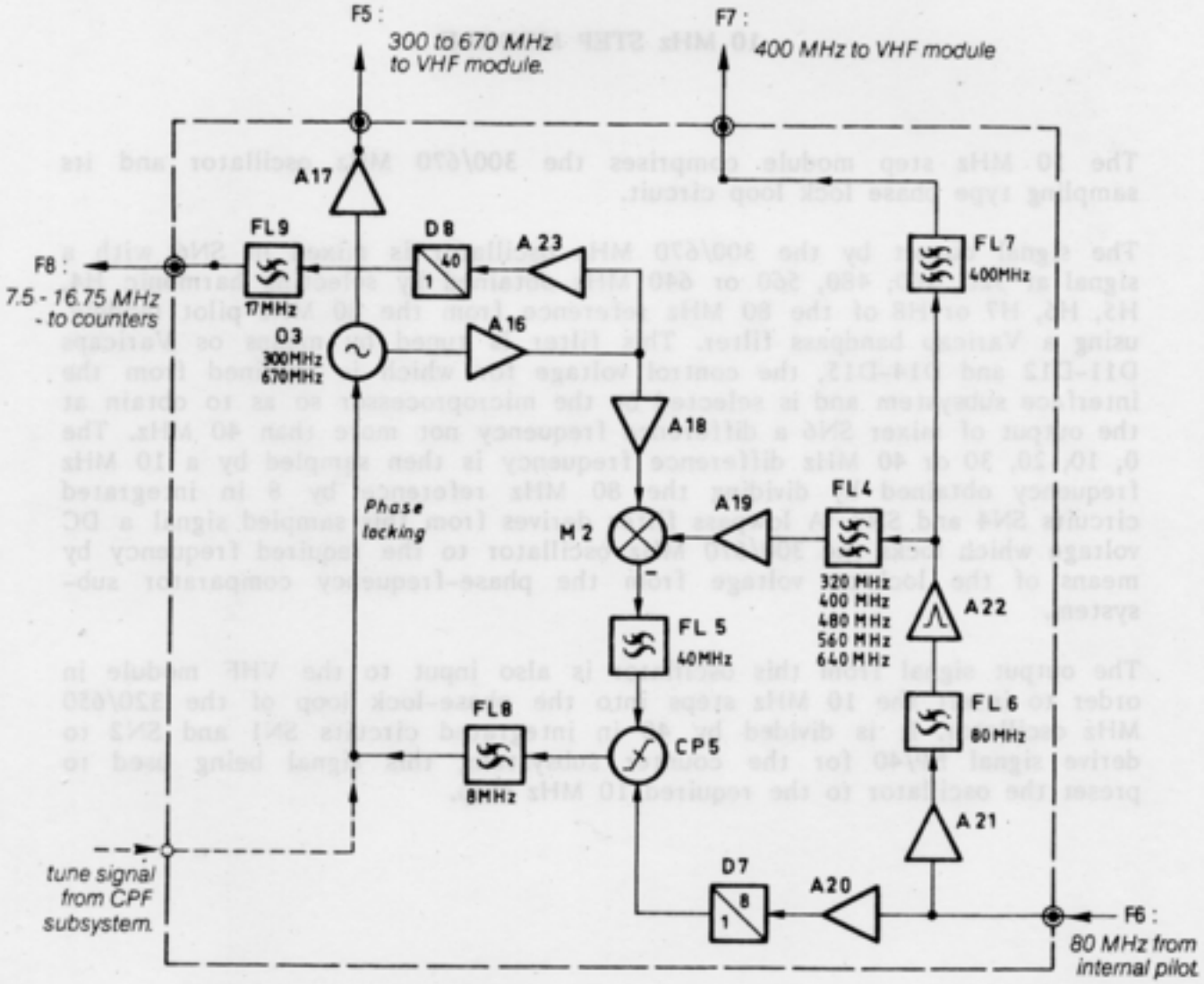
10 MHz STEP MODULE

The 10 MHz step module comprises the 300/670 MHz oscillator and its sampling type phase lock loop circuit.

The signal output by the 300/670 MHz oscillator is mixed in SN6 with a signal at 320, 400, 480, 560 or 640 MHz obtained by selecting harmonic H4, H5, H6, H7 or H8 of the 80 MHz reference from the 80 MHz pilot module, using a Varicap bandpass filter. This filter is tuned by means os Varicaps D11-D12 and D14-D15, the control voltage for which is obtained from the interface subsystem and is selected by the microprocessor so as to obtain at the output of mixer SN6 a difference frequency not more than 40 MHz. The 0, 10, 20, 30 or 40 MHz difference frequency is then sampled by a 10 MHz frequency obtained by dividing the 80 MHz reference by 8 in integrated circuits SN4 and SN7. A lowpass filter derives from this sampled signal a DC voltage which locks the 300/670 MHz oscillator to the required frequency by means of the lock-on voltage from the phase-frequency comparator sub-system.

The output signal from this oscillator is also input to the VHF module in order to insert the 10 MHz steps into the phase-lock loop of the 320/650 MHz oscillator. It is divided by 40 in integrated circuits SN1 and SN2 to derive signal FP/40 for the counter subsystem, this signal being used to preset the oscillator to the required 10 MHz step.

BLOCK DIAGRAM



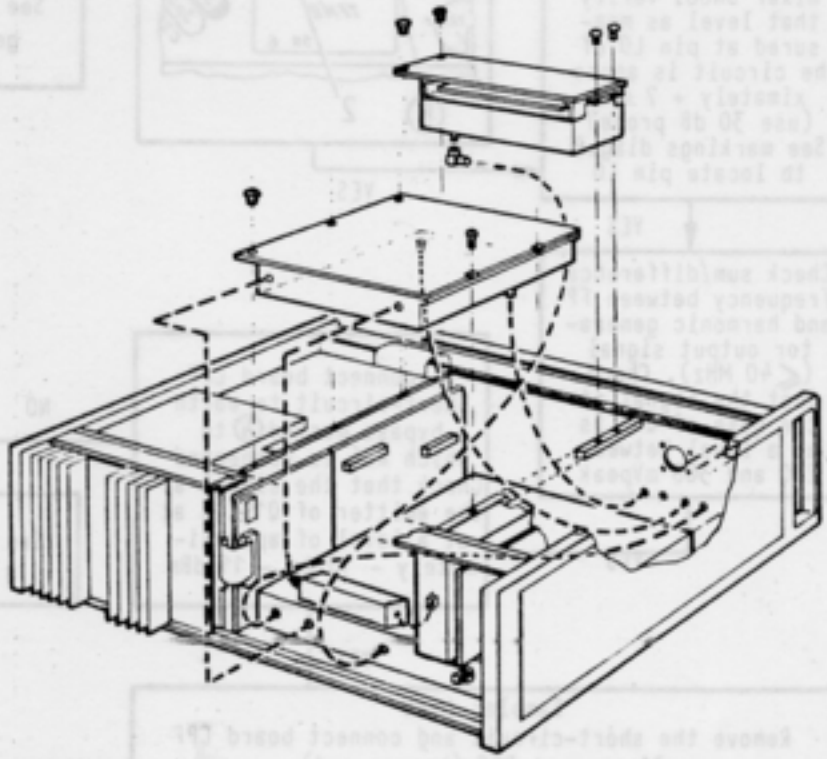
CONNECTOR PIN-OUT

Tune voltage FP from phase-frequency comparators.....	3	
320-650 MHz oscillator tune loop enable signal from phase-frequency comparators.....	4	
FP/40 signal detected level to interface module (level 4).....	13	
Connected to pin 4.....	15	
Level detection : 400 MHz to interface (level 5).....	16	
Level detection : FP to interface module (level 6).....	17	
Reference frequency tuning signal from interface.....	18	
400 MHz enable signal from interface.....	19	
+ 18 V.....	7	14
+ 12 V.....	8	9
+ 5 V.....	10	
- 12 V.....	11	12
⏚	5	6
Pins not listed not connected.....	NC	

MODULE TESTS

Preparation

- Remove the bottom panel from the instrument
- Remove all fixing screws from the silk-screened cover (027141) and remove the cover to gain access to the circuit components



TROUBLESHOOTING CHARTS

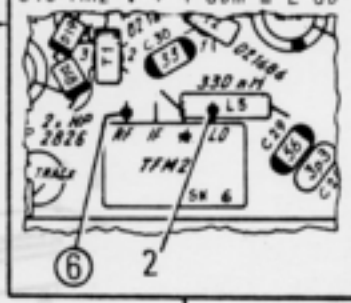
Fine loop test
(10 MHz step module)

Check 80 MHz oscillator lock-on loop
Check level at measurement point ① is between 3 and 9 V

NO → See 80-10 MHz **pilot** module

YES →

Test level of 320, 400, 480, 560 and 640 MHz harmonics at measurement point ⑥
320 MHz : + 1 dBm ± 1 dB
400 MHz : + 3 dBm ± 2 dB
480 MHz : + 4 dBm ± 2 dB
560 MHz : + 4 dBm ± 2 dB
640 MHz : + 4 dBm ± 2 dB



NO → See harmonics generator

YES →

Test signal on second input of mixer SN06. Verify that level as measured at pin LO of the circuit is approximately + 7 dBm (use 30 dB probe)
See markings diag.2 to locate pin LO

NO → See amplifier circuit Q13, Q12, Q09

YES →

Check sum/difference frequency between FP and harmonic generator output signal (≤ 40 MHz). Check that the signal at the base of Q16 is at a level between 200 and 300 mVpeak

NO → See mixer or filter

YES →

Disconnect board CPF
Short-circuit to earth bypass marked ④ to which R86 is connected
Check that the signal at the emitter of Q19 is at at a level of approximately - 10 to - 11 dBm

NO → See divide by 8 circuit

YES →

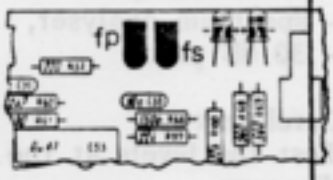
Sampler test
Remove the short-circuit and connect board CPF
Disconnect R52 (bypass end)
Rotate P1 to obtain 0 V at measurement point ⑦
Disconnect R99 and R62 and verify lock-on voltage at common point of R56 and R57 (approximately - 0.4 V)
Connect R62, disconnect R62 and verify that lock-voltage is 18 V. Reconnect R99, R63 and R52

NO → See sampler

YES → See low-pass filter FL8

Check the 300-670 MHz oscillator phase-lock loop

Short-circuit to earth point FP on the phase-frequency comparator board CPF



Connect a spectrum analyser to the output the module and check that the signal obtained is correct

YES → Fine loop fault Test after removing the short-circuit from board CPF

NO → **Tune loop test**

10 MHz step module Check that the voltage at terminals of R52 is null (0V)

NO → Leakage (sampler or oscillator)

YES →

10 MHz step module Test operation of divide by 40 circuit by monitoring frequency FP(300-670 MHz) and divided signal (FP/40) outputs of module

NO → See oscillator and divide by 40 circuit

YES →

Counter board Test for presence of FP/40 at collector of Q10 (amplifier)

NO → See input amplifier (Q9 and Q10)

YES →

Board CPF (comparators). Check the division ratio of the divide by 30 to 69 circuit at pin 1 of SN18. Set 420 MHz The division ratio should be 40

NO → See 30 to 69 divider on counter board

YES →

Board CPF Test operation of fine tune (FP) comparator. Disconnect FP/40 coaxial connection to counters board. Check that the FP lock-on voltage is 18 V on bypass marked (3) (10 MHz step module)

NO → See comparator (fine tune pull up voltage)

YES →

Board CPF. Make FP/40 connection and short-circuit package of transistors Q21 and Q22 (cancels reference 4 MHz). Check voltage measured at bypass 3 is approximately 0.3 V

NO → See comparator (fine tune pull-up voltage)

YES →

Remove short-circuit from board CPF

ADJUSTMENTS

MODULE REPAIRED

Equipment required :
- multimeter,
- spectrum analyser,
- 30 dB probe

1) Level test

Test the levels at the measurement points indicated on the electrical circuit diagram

a) 80 MHz input, measurement point (1) : + 1 dBm ± 1 dB
b) Divide by 8 input, measurement point (2) : - 2 dBm ± 1 dB
c) Divide by 8 output, measurement point (3) : - 11 dBm ± 1 dB
(10 - 40 MHz spectrum)
d) Harmonic generator input, measurement point (4) : + 13 dBm ± 2 dBm
(C58 set to maximum value)
e) Harmonic generator, measurement point (5) : - 2 dBm ± 5 dB
(between 320 and 640 MHz)

2) 400 MHz output

a) Set frequency below 80 MHz and connect analyser to 400 MHz output
b) Adjust C53 to obtain maximum level - 1 dBm ± 1 dB.
Avoid tuning to adjacent frequency component
c) If necessary adjust the output winding tapping point to obtain the correct level
d) Set a frequency exceeding 80 MHz and check that the signal attenuation is

3) Mixer tracking filter

a) Disconnect resistor R3, 300 - 670 MHz oscillator and set frequency 640 MHz (non-doubled range)
b) Connect spectrum analyser to measurement point (6) using 30 dB probe
c) Adjust potentiometer P1 on interface cable and variable capacitor C34 of module to obtain maximum harmonic level (+ 4 dBm ± 2 dB)
d) Set frequency 560 MHz and adjust potentiometer P2 to obtain maximum harmonic level (+ 4 dBm ± 2 dB)
e) Set 480 MHz and adjust P3
(+ 4 dBm ± 2 dB)
f) Set 400 MHz and adjust P4
(+ 3 dBm ± 2 dB)
g) Set 328 MHz and adjust P5
(+ 1 dBm ± 1 dB)
Adjust R49 if necessary
h) Reconnect resistor R3

4) 300 - 670 MHz oscillator

a) Connect the spectrum analyser to the 300 - 670 MHz output
b) Rotate the front panel main frequency control and confirm that the oscillator covers the band
c) Check that the minimum and maximum levels across the range correspond to + 6 and + 8 dBm, respectively
Adjust R3 if necessary
d) Set 320 MHz ; Varicap voltage should be $\geqslant$ 0.5 V
Set 349 MHz ; Varicap voltage should be $\leqslant$ 15 V
e) Measure harmonic 2 and levels under worst case conditions : H2 $\geqslant$ 16 dB, H3 $\geqslant$ 20 dB

5) Oscillator lock-on

a) Set oscillator to 670 MHz using front panel frequency spinwheel
b) Rotate potentiometer P01 of the sampler to the left and then to the right, measuring at point (7) the voltages corresponding to desynchronisation of the loop
To left V1 $\geqslant$ + 50 mV
To right V2 $\leqslant$ - 150 mV
Adjust P01 to obtain (V2 + V1)/2 at point (7) (generally ± 80 mV)
c) Check that the 300 - 670 MHz range is covered in steps of 10 MHz
d) Set oscillator to 670 MHz (FO)
Adjust C40 to have minimum components at 10 MHz of FO ($\leqslant$ - 75 dB)
Adjust C36 to have minimum components at 20 MHz of FO ($\leqslant$ - 85 dB)
Check that the components between 30 and 100 MHz of FO are $<$ - 85 dB

6) FP/40 divider

a) Measure 5 or 6.8 V ± 0.2 V at measurement point (8)
b) Measure level at measurement point (9) using analyser and 30 dB probe (- 3 dBm $<$ N $<$ + 4 dBm) then at 7.5 - 16.75 MHz output (- 5 dBm ± 1)

7) Test points

Measure the following voltages :

LEV 16 : 400 MHz output, for set frequency below 80 MHz - 0.1 V $<$ U $<$ + 0.1 V
LEV 17 : FP output (300 - 670 MHz) : - 1 V $<$ U $<$ - 0.4 V
LEV 13 : FP/40 output (7.5 - 16.75 MHz) + 0.1 V $<$ U $<$ + 0.25 V

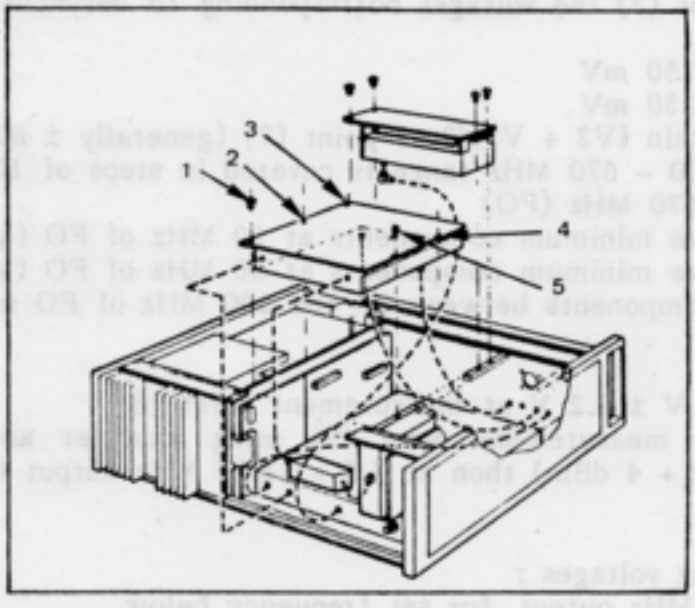
8) Noise measurement

a) Set 649 MHz and verify that noise level at 600 kHz is - 135 dB ± 2
b) Set 320 MHz and verify that noise level is - 138 dB ± 2

REMOVING AND REPLACING THE MODULE

REPLACING THE MODULE

a) Remove the bottom panel and the rear panel from the instrument
b) Unscrew and remove the rigid coaxial connections between the VHF and MHz step modules (see diagram)
c) Remove the two attachment screws marked on the diagram and lift out the module. Unscrew the two coaxial connections to the base of the module
d) Remove the module and replace by carrying out the operations described for removal in reverse order

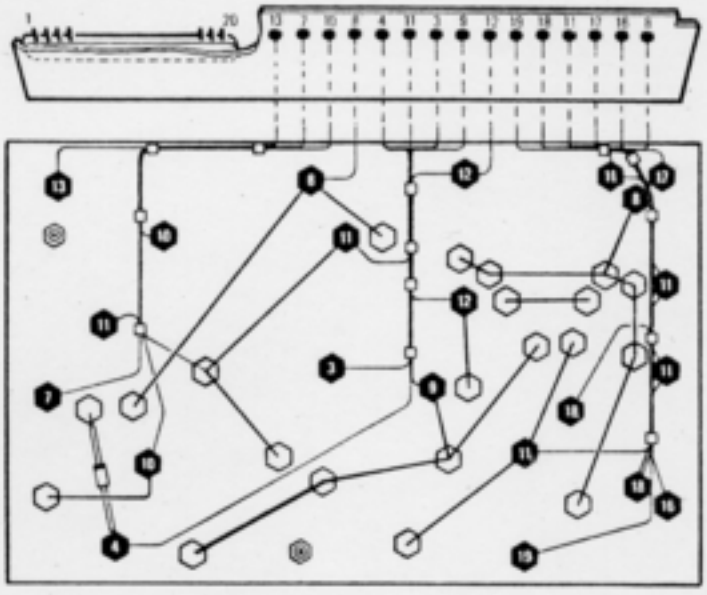


CALIBRATING THE MODULE (module replaced or not)

1) Mixer input
a) Open up the module
b) Connect the spectrum analyser to measurement point (6) on the circuit using the 30 dB probe
c) Set 640 MHz (CW mode)
Adjust capacitor C34 to obtain maximum level at measurement point

2) 80 MHz pilot harmonics

The levels of harmonics 320, 400, 480, 560 and 640 MHz are adjusted on the interface board. Refer to the section of this chapter on this subsystem



VHF MODULE

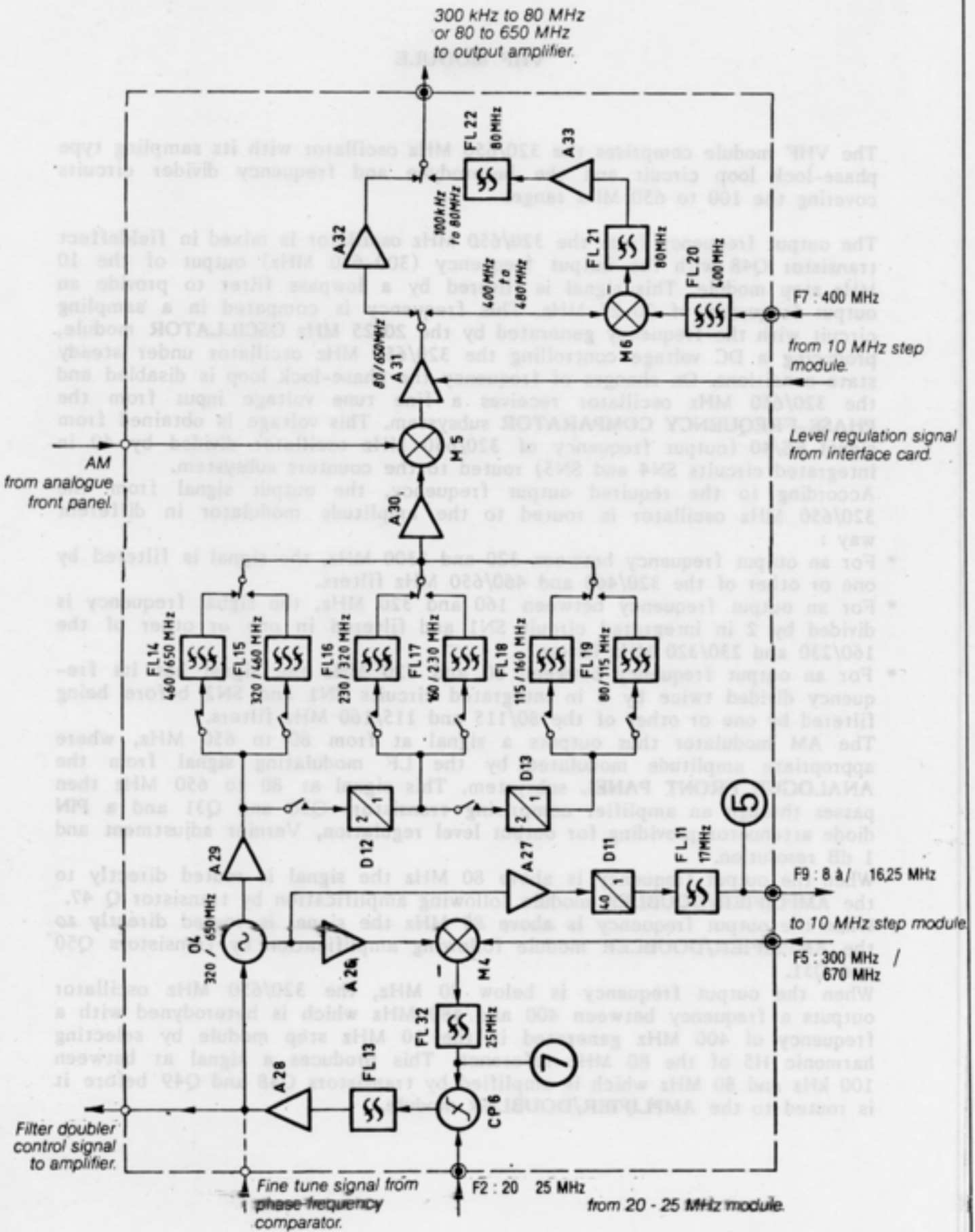
The VHF module comprises the 320/650 MHz oscillator with its sampling type phase-lock loop circuit and the heterodyne and frequency divider circuits covering the 100 to 650 MHz range.

The output frequency from the 320/650 MHz oscillator is mixed in fieldeffect transistor Q48 with the output frequency (300-670 MHz) output of the 10 MHz step module. This signal is filtered by a lowpass filter to provide an output frequency of 20-25 MHz. This frequency is compared in a sampling circuit with the frequency generated by the **20/25 MHz OSCILLATOR** module, producing a DC voltage controlling the 320/650 MHz oscillator under steady state conditions. On changes of frequency the phase-lock loop is disabled and the 320/650 MHz oscillator receives a fine tune voltage input from the **PHASE-FREQUENCY COMPARATOR** subsystem. This voltage is obtained from signal FS/40 (output frequency of 320/650 MHz oscillator divided by 40 in integrated circuits SN4 and SN5) routed to the counters subsystem.
According to the required output frequency, the output signal from the 320/650 MHz oscillator is routed to the amplitude modulator in different way :

- For an output frequency between 320 and 1300 MHz, the signal is filtered by one or other of the 320/460 and 460/650 MHz filters.
- For an output frequency between 160 and 320 MHz, the signal frequency is divided by 2 in integrated circuit SN1 and filtered in one or other of the 160/230 and 230/320 MHz filters.
- For an output frequency between 80 and 320 MHz the signal has its frequency divided twice by 2 in integrated circuits SN1 and SN2 before being filtered by one or other of the 80/115 and 115/160 MHz filters.

The AM modulator thus outputs a signal at from 80 to 650 MHz, where appropriate amplitude modulated by the LF modulating signal from the **ANALOGUE FRONT PANEL** subsystem. This signal at 80 to 650 MHz then passes through an amplifier comprising transistors Q30 and Q31 and a **PIN** diode attenuator providing for output level regulation, Vernier adjustment and 1 dB resolution.
When the output frequency is above 80 MHz the signal is routed directly to the **AMPLIFIER/DOUBLER** module following amplification by transistor Q 47.
When the output frequency is above 80 MHz the signal is routed directly to the **AMPLIFIER/DOUBLER** module following amplification by transistors Q50 and Q51.
When the output frequency is below 80 MHz, the 320/650 MHz oscillator outputs a frequency between 400 and 480 MHz which is heterodyned with a frequency of 400 MHz generated in the 10 MHz step module by selecting harmonic H5 of the 80 MHz reference. This produces a signal at between 100 kHz and 80 MHz which is amplified by transistors Q48 and Q49 before it is routed to the **AMPLIFIER/DOUBLER** module.

BLOCK DIAGRAM



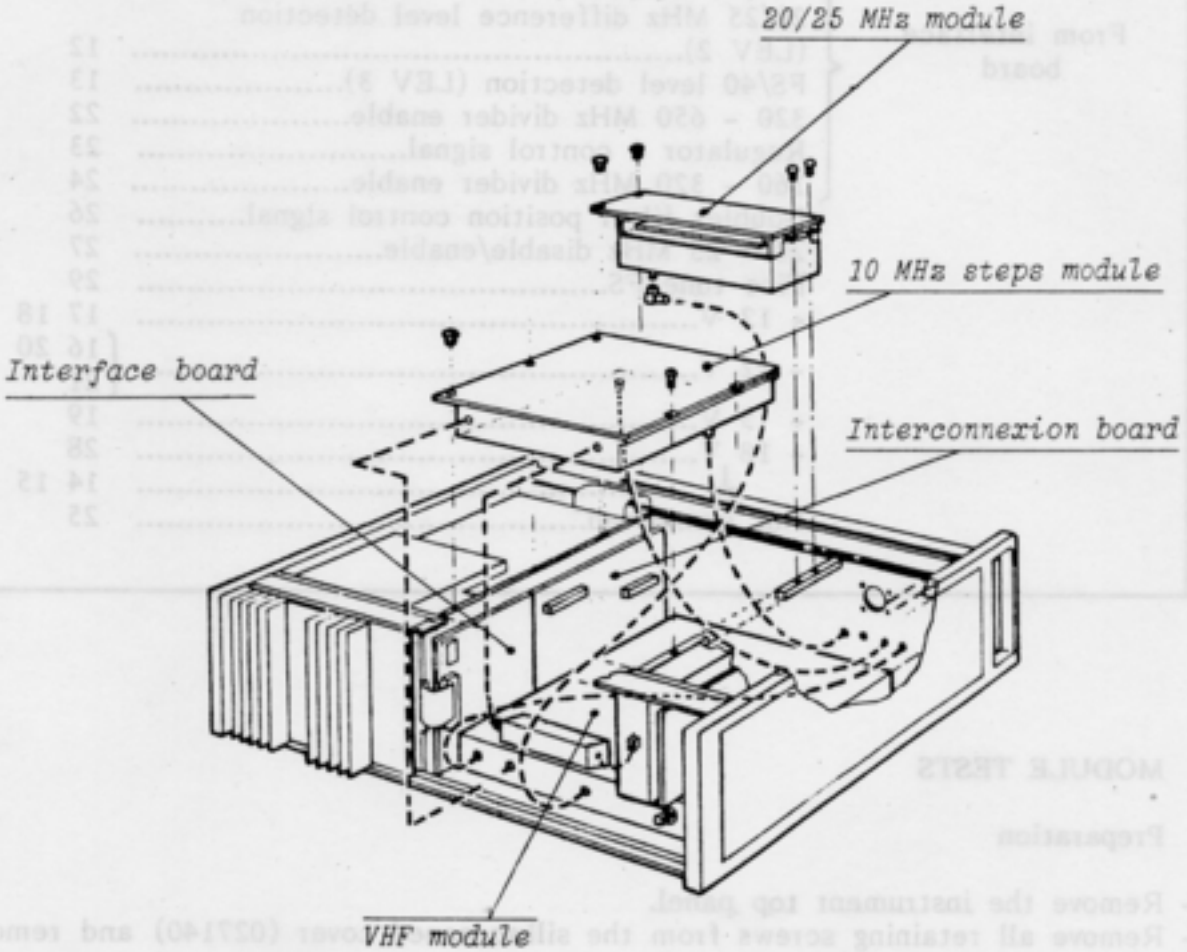
CONNECTOR PIN-OUT

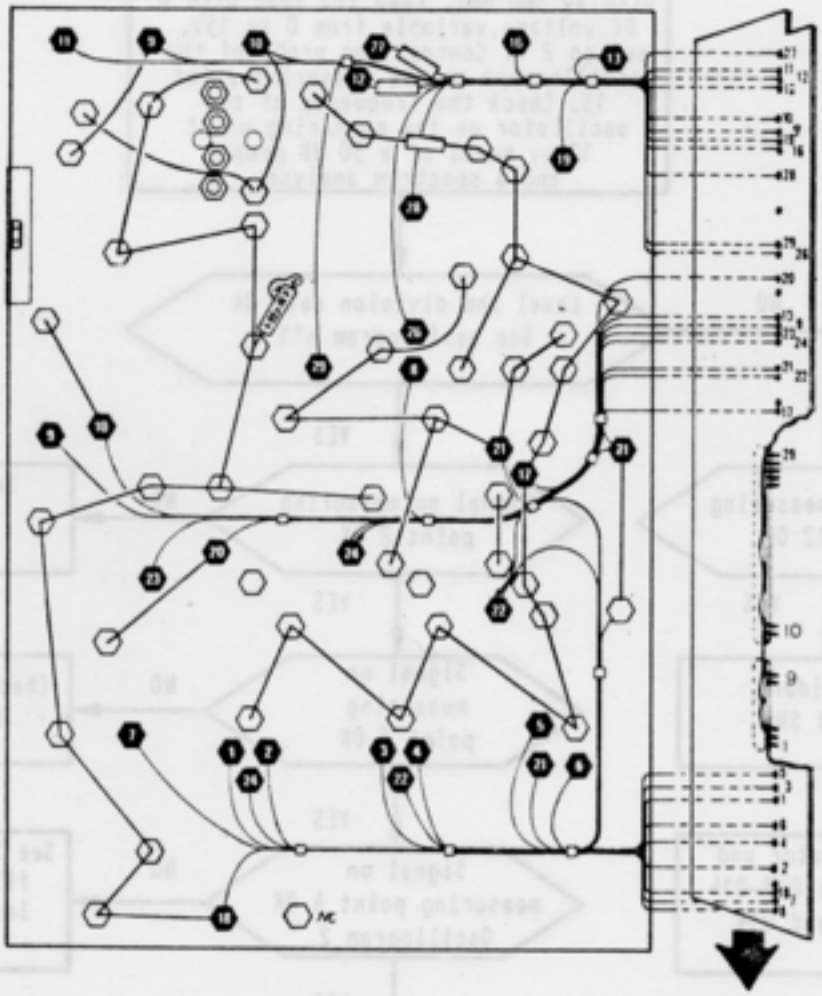
From interface board	80/115 MHz filter enable	1
	115/160 MHz filter enable	2
	160/230 MHz filter enable	3
	230/320 MHz filter enable	4
	320/460 MHz filter enable	5
	460/650 MHz filter enable	6
	AM from analogue front panel	7
	FM 300 kHz from interface board	8
	80/650 MHz output enable signal from interface board	9
From interface board	0/80 MHz output enable	10
	Output frequency level detection (LEV 1)	11
	20/25 MHz difference level detection (LEV 2)	12
	FS/40 level detection (LEV 3)	13
	320 - 650 MHz divider enable	22
	Regulator 1 control signal	23
	160 - 320 MHz divider enable	24
	Doubler filter position control signal	26
	20 - 25 MHz disable/enable	27
	Fine tune FS	29
	+ 12 V	17 18
	- 12 V	16 20 21
	+ 5 V	19
	+ 18 V	28
	⏚	14 15
	Not connected	25

MODULE TESTS

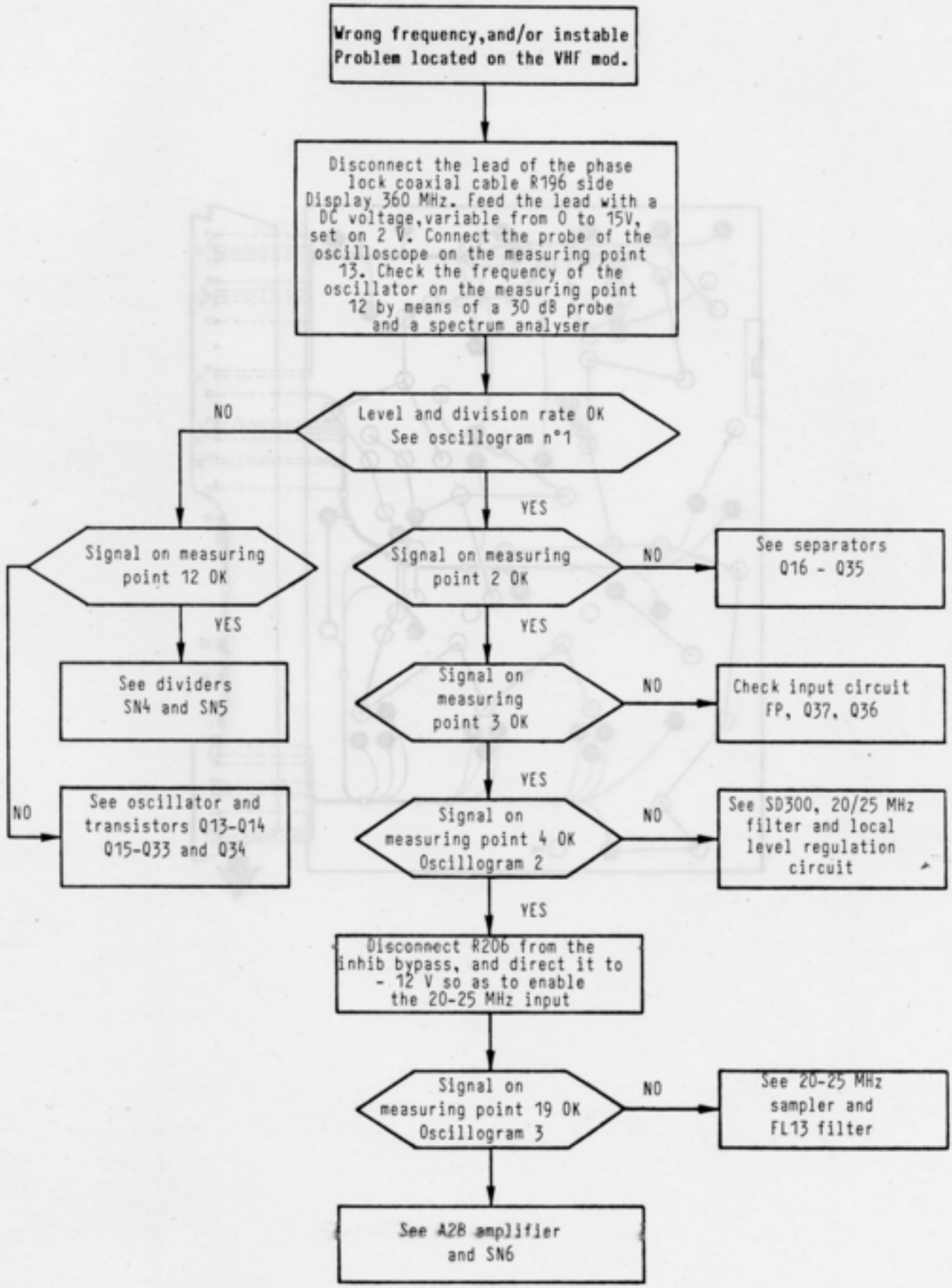
Preparation

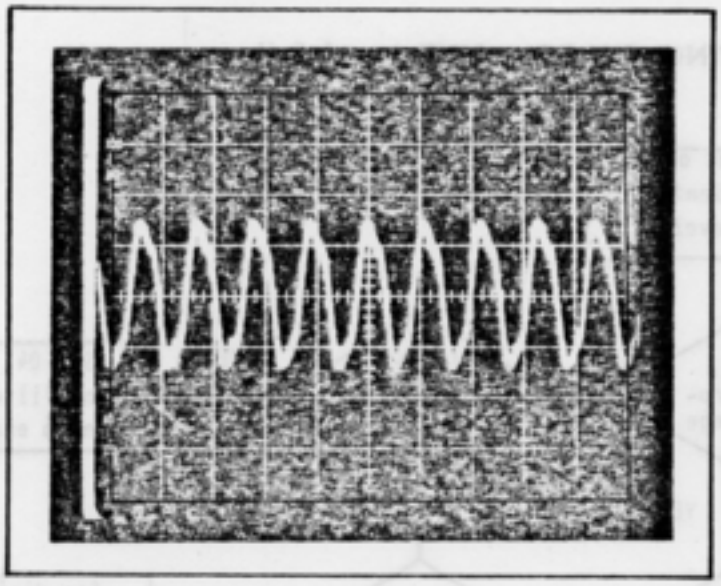
- Remove the instrument top panel.
- Remove all retaining screws from the silkscreened cover (027140) and remove cover to gain access to components.


20/25 MHz module
10 MHz steps module
Interface board
Interconnexion board
VHF module

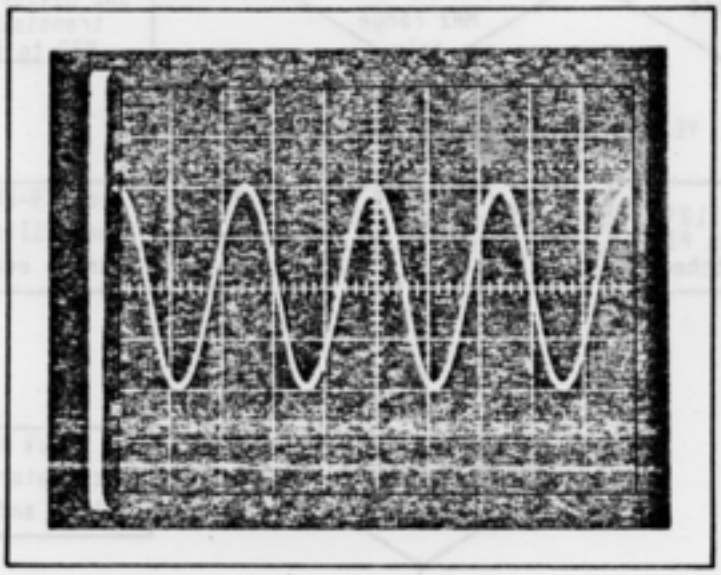


TROUBLESHOOTING CHART – VHF Frequency failure

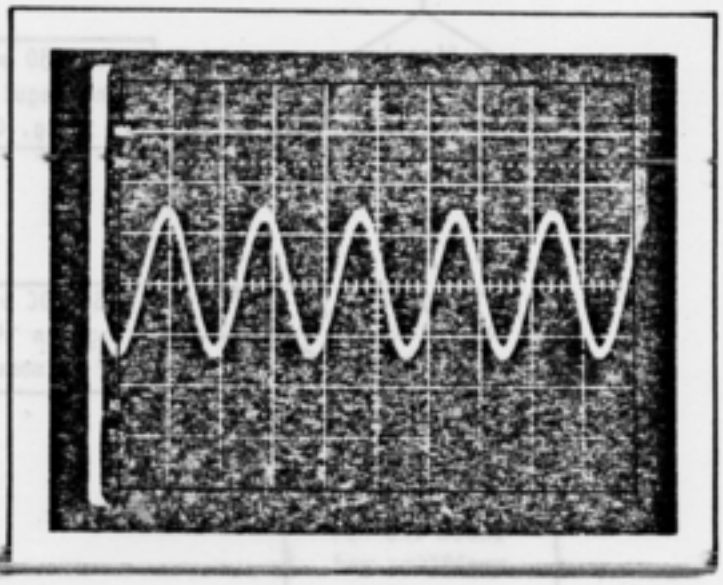




Oscillogram n°1
FS/40 output
Oscillator frequency
360 MHz
0.2V/div
0.1µs/div

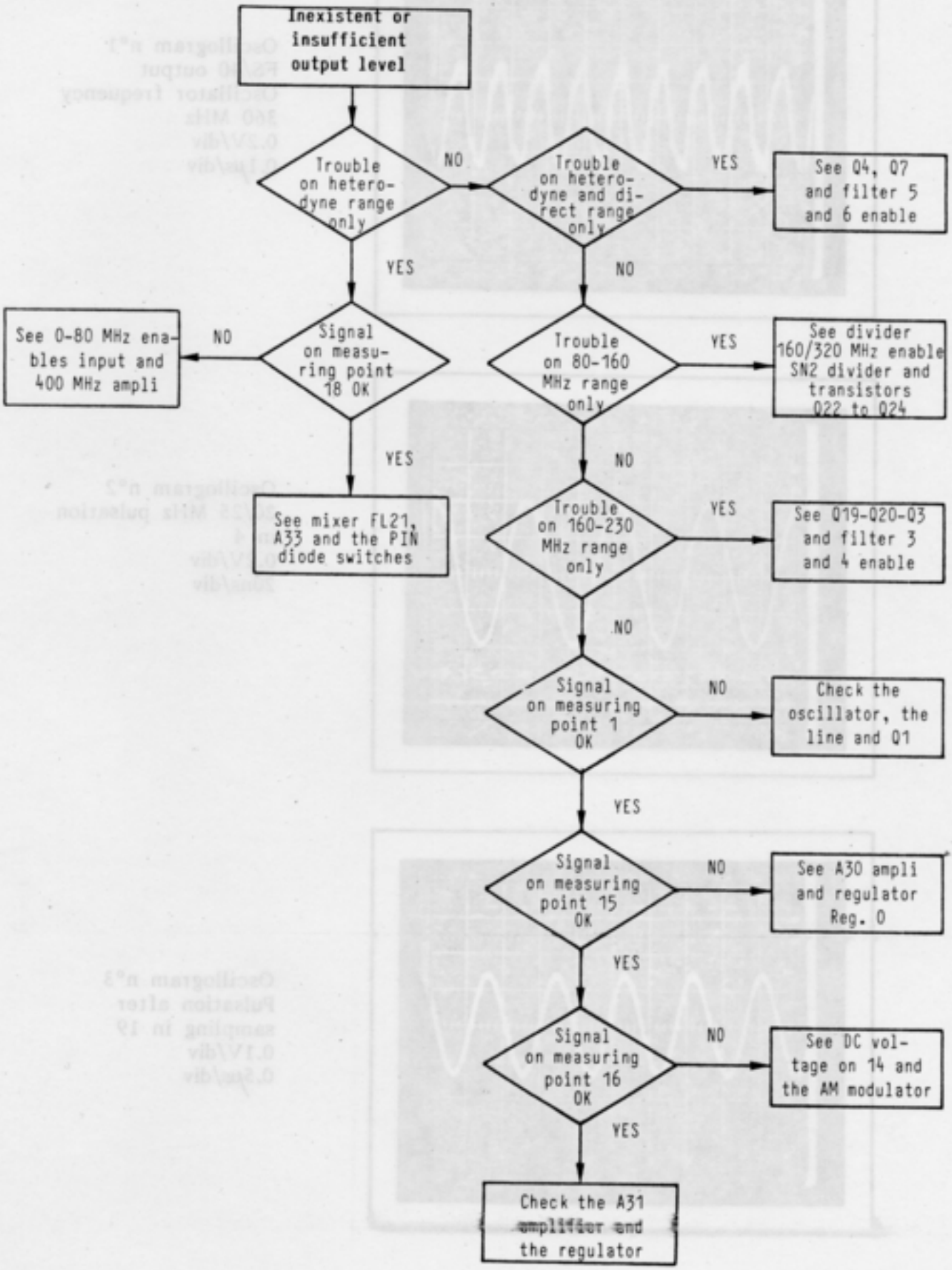


Oscillogram n°2
20/25 MHz pulsation
in 4
0.2V/div
20ns/div



Oscillogram n°3
Pulsation after
sampling in 19
0.1V/div
0.5µs/div

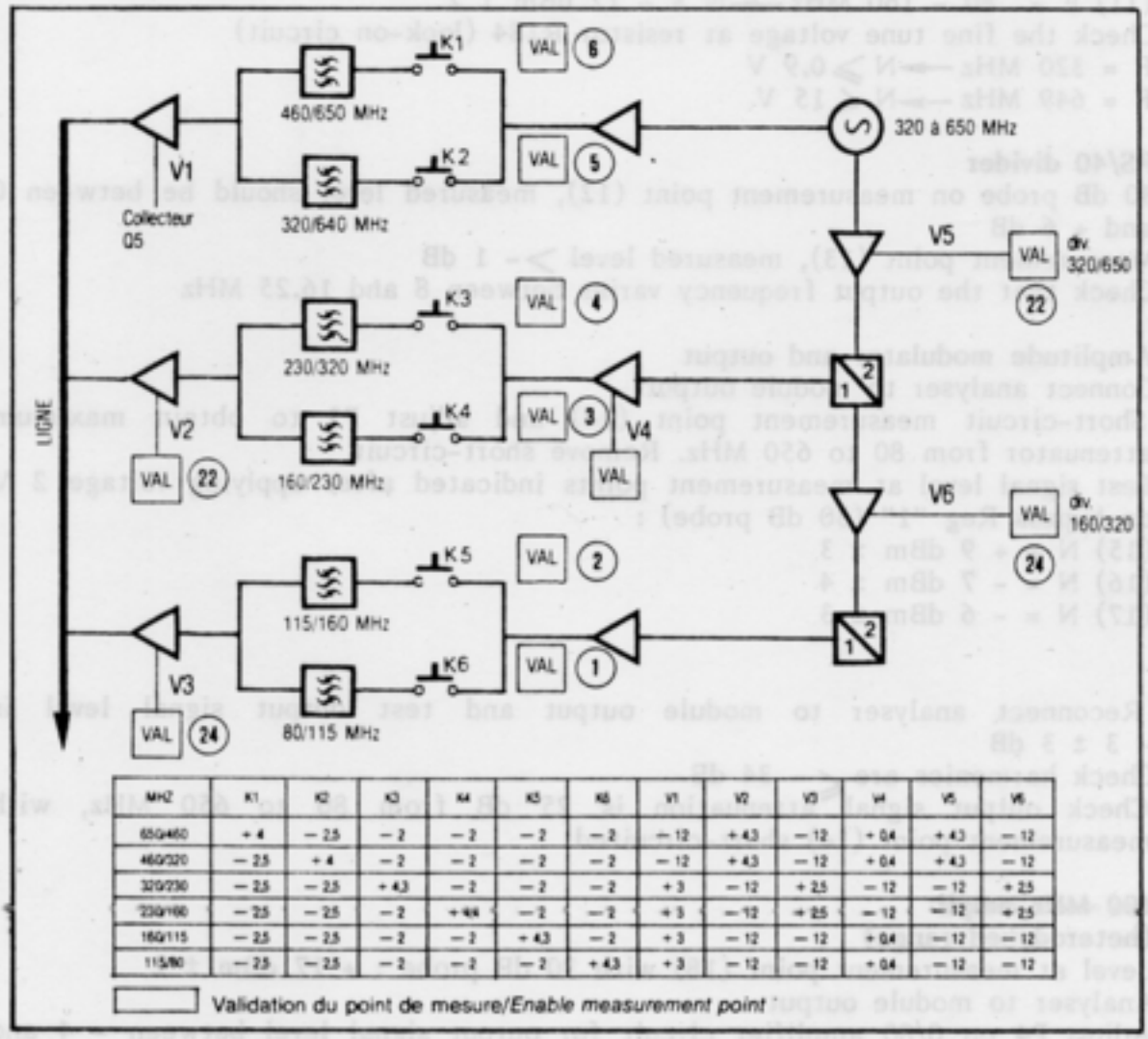
TROUBLESHOOTING CHART - VHF Level failure



ADJUSTMENTS
MODULE REPAIRED

Equipment required :
- spectrum analyser + 30 dB probe
- multimeter

1) Enable dividers and range filters
Test the DC voltages at points marked on the diagram and in the table below :



MHZ	K1	K2	K3	K4	K5	K6	V1	V2	V3	V4	V5	V6
650/460	+ 4	− 2,5	− 2	− 2	− 2	− 2	− 12	+ 4,3	− 12	+ 0,4	+ 4,3	− 12
460/320	− 2,5	+ 4	− 2	− 2	− 2	− 2	− 12	+ 4,3	− 12	+ 0,4	+ 4,3	− 12
320/230	− 2,5	− 2,5	+ 4,3	− 2	− 2	− 2	+ 3	− 12	+ 2,5	− 12	− 12	+ 2,5
230/160	− 2,5	− 2,5	− 2	+ 4,3	− 2	− 2	+ 3	− 12	+ 2,5	− 12	− 12	+ 2,5
160/115	− 2,5	− 2,5	− 2	− 2	+ 4,3	− 2	+ 3	− 12	− 12	+ 0,4	− 12	− 12
115/80	− 2,5	− 2,5	− 2	− 2	− 2	+ 4,3	+ 3	− 12	− 12	+ 0,4	− 12	− 12

Validation du point de mesure/*Enable measurement point*

2) Oscillator and phase-lock loop test
a) Plug in all external connections to module
b) Use analyser and 30 dB probe to test output level of oscillator and at measurement point (1) is between - 3 and + 6 dBm

c) Test oscillator lock-on and levels of signals at measurement points indicated (use 30 dB probe) :

(2) for F = 320 MHz → N = + 12 dBm ± 3
for F = 650 MHz → N = + 20 dBm ± 3
(3) for F = 300 MHz → N = + 10 dBm ± 2
for F = 670 MHz → N = + 16 dBm ± 3
(4) for F = 320 MHz → N = + 5 dBm ± 2
for F = 650 MHz → N = + 11 dBm ± 2
(5) N = + 10 dBm ± 1

d) Measure the maximum signal levels at the following measurement points :

(8) F = 320 - 650 MHz → N = + 5 dBm ± 3
(9) F = 160 - 320 MHz → N = + 12 dBm ± 2
(10) F = 160 - 320 MHz → N = + 3 dBm ± 3
(11) F = 80 - 160 MHz → N = + 12 dBm ± 2

e) Check the fine tune voltage at resistor R184 (lock-on circuit)
F = 320 MHz → N $\geqslant$ 0.9 V
F = 649 MHz → N $<$ 15 V

3) FS/40 divider

a) 30 dB probe on measurement point (12), measured level should be between 0 and + 6 dB
b) Measurement point (13), measured level $>$ - 1 dB
c) Check that the output frequency varies between 8 and 16.25 MHz

4) Amplitude modulator and output

a) Connect analyser to module output
b) Short-circuit measurement point (14) and adjust P3 to obtain maximum attenuator from 80 to 650 MHz. Remove short-circuit
c) Test signal level at measurement points indicated after applying voltage 2 V on bypass Reg "1" (30 dB probe) :

(15) N = + 9 dBm ± 3
(16) N = - 7 dBm ± 4
(17) N = - 6 dBm ± 3

d) Reconnect analyser to module output and test output signal level is - 3 ± 3 dB
e) Check harmonics are $\leqslant$ - 34 dB
f) Check output signal attenuation is 25 dB from 80 to 650 MHz, with measurement point (14) short-circuited

5) 400 MHz ampli (heterodyned range)

a) Level at measurement point (18) with 30 dB probe : + 17 dBm ± 2
b) Analyser to module output
Adjust P4 on 0/80 amplifier circuit for output signal level between - 4 and - 10 dBm from 300 kHz to 80 MHz
c) Check that harmonics are $<$ - 35 dB for output frequencies from 1 to 80 MHz

6) Noise level

a) Connect analyser to module output
b) Set oscillator to 320 MHz (downward mode)
c) Check that noise level is $\leqslant$ - 137 dB at 600 kHz from carrier
d) Set oscillator to 649 MHz, carrier noise level at 600 kHz should be $\leqslant$ - 133dB

7) Noise floor

Use the spectrum analyse to verify that the wideband noise floor is - 145 dB in the 80 - 650 MHz range and - 142 dB in the heterodyned range

8) Non-harmonic components (module closed)

Set the oscillator to the heterodyned range 300 kHz to 80 MHz and verify that the components at 400 and 800 MHz of Fo are - 80 dB and that the absolute component at 80 MHz is $\leqslant$ - 100 dB

REMOVING AND REPLACING THE MODULE

a) Remove the righthand side panel (meter side) and rear panel
b) Unscrew and remove the rigid coaxial connections on the VHF module
c) Remove the lateral attachments and the six retaining screws on the top part of the module (see diagram)
d) Raise and pull out the module, avoiding impact with adjacent subsystems
e) Follow the reserve procedure to replace the module
Lateral attachments-connecting wire bundle-from front panel

CALIBRATING THE MODULE
(module replaced or not)

See chapter **CALIBRATION**

TEST POINTS ACCESSIBLE ON TOP OF MODULE

1) Oscillator lock-on :
1 - 81 MHz ≃ 3.32 V - 6.03 V
82 - 162 MHz ≃ 1.21 V - 13.36 V
163 - 324 MHz ≃ 1.16 V - 13.36 V
325 - 650 MHz ≃ 1.14 V - 13.43 V

2) Frequency doubler
Tracking filter control voltage : same values as under (1) above

3) 20 - 25 MHz disable :
≃ - 12 V when oscillator locked on
≃ + 0.35 V when signal absent

4) 160/320 MHz divider :
1 - 162 MHz ≃ - 12 V
163 - 324 MHz ≃ + 2.55 V
325 - 650 MHz ≃ - 12 V

5) VHF and amplifier regulation
≃ 2 - 3 V, according to frequency

6) 320/650 MHz divider :
80 - 324 MHz ≃ - 12 V
325 - 650 MHz ≃ + 3.1 V

7) 0/80 MHz range :
1 - 81 MHz ≃ - 12 V
81 - 650 MHz ≃ + 1.6 V

8) 80/650 MHz range :
1 - 81 MHz ≃ + 1.7 V
81 - 650 MHz ≃ - 12 V

9) Modulating reference :
+ 2.5 V (DC)

10) 460/650 MHz filter operating voltage :
1 - 50 MHz ≃ - 2.97 V
60 - 81 MHz ≃ + 3.58 V
82 - 459 MHz ≃ - 2.97 V
460 - 650 MHz ≃ + 3.59 V

11) 320/460 MHz filter operating voltage :

1 - 59 MHz ≃ + 3.56 V
60 - 324 MHz ≃ - 2.96 V
325 - 459 MHz ≃ + 3.56 V
460 - 650 MHz ≃ - 2.97 V

12) 230/320 MHz filter operating voltage :

1 - 229 MHz ≃ - 2.49 V
230 - 324 MHz ≃ + 4.02 V
325 - 650 MHz ≃ - 2.49 V

13) 160/320 MHz filter operating voltage :

1 - 162 MHz ≃ - 2.48 V
163 - 229 MHz ≃ + 4.11 V
230 - 650 MHz ≃ - 2.48 V

14) 115/160 MHz filter operating voltage :

1 - 114 MHz ≃ - 2.47 V
115 - 162 MHz ≃ + 4.07 V
163 - 650 MHz ≃ - 2.47 V

15) 80/115 MHz filter operating voltage :

1 - 81 MHz ≃ - 2.47 V
82 - 114 MHz ≃ + 4.07 V
115 - 650 MHz ≃ - 2.48 V

OUTPUT MODULE

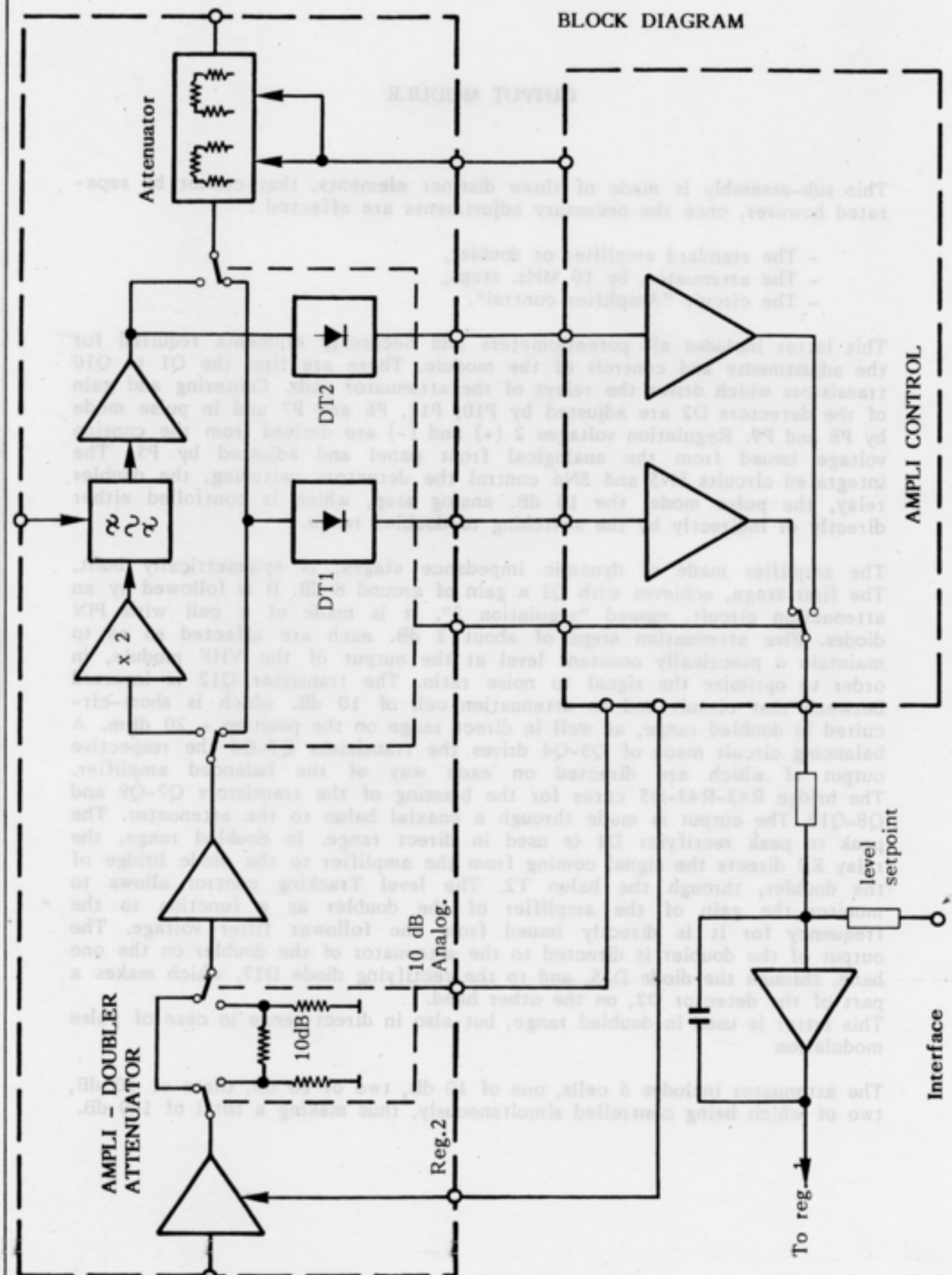
This sub-assembly is made of three distinct elements, that cannot be separated however, once the necessary adjustments are effected :

- The standard amplifier or doubler,
- The attenuator, by 10 MHz. steps,
- The circuit "Amplifier control".

This latter includes all potentiometers and necassary elements required for the adjustments and controls of the module. There are first the Q1 to Q10 transistors which drives the relays of the attenuator pads. Centering and gain of the detectors D2 are adjusted by P10, P11, P6 and P7 and in pulse mode by P8 and P9. Regulation voltages 2 (+) and (-) are derived from the consign voltage issued from the analogical front panel and adjusted by P5. The integrated circuits SN5 and SN6 control the detectors switching, the doubler relay, the pulse mode, the 10 dB. analog step, which is controlled either directly or indirectly by the switching to doubled range.

The amplifier made of dynamic impedance stages, is symmetrically built. The first stage, achieves with Q1 a gain of around 8 dB. It is followed by an attenuation circuit, named "regulation 2". It is made of a cell with PIN diodes. Five attenuation steps of about 2 dB. each are affected so as to maintain a practically constant level at the output of the VHF module, in order to optimize the signal to noise ratio. The transistor Q12 is inserted between that circuit and an attenuation cell of 10 dB. which is short-circuited in doubled range, as well in direct range on the position + 20 dBm. A balancing circuit made of Q3-Q4 drives the transistors Q5-Q6 the respective output of which are directed on each way of the balanced amplifier. The bridge R42-R43-D5 cares for the biassing of the transistors Q7-Q9 and Q8-Q10. The output is made through a coaxial balun to the attenuator. The peak to peak rectifyier D1 is used in direct range. In doubled range, the relay K2 directs the signal coming from the amplifier to the diode bridge of the doubler, through the balun T2. The level Tracking control allows to monitor the gain of the amplifier of the doubler as a function to the frequency for it is directly issued from the follower filter voltage. The output of the doubler is directed to the attenuator of the doubler on the one hand, through the diode D15, and to the rectifying diode D17, which makes a part of the detector D2, on the other hand.
This latter is used in doubled range, but also in direct range in case of pulse modulation

The attenuator includes 6 cells, one of 10 dB, two of 20 dB, three of 30 dB, two of which being controlled simultaneously, thus making a total of 140 dB.


BLOCK DIAGRAM
Attenuator
DT2
DT1
x 2
AMPLI CONTROL
level setpoint
10 dB Analog.
10dB
AMPLI - DOUBLER ATTENUATOR
Reg.2
To reg
Interface

CONNECTOR PIN-OUT

To attenuator	- 60 dB pad control signal	1
	- 30 dB pad control signal	2
	- 20 dB pad control signal	3
	- 20 dB pad control signal	4
	- 10 dB pad control signal	5
	+ 12 V	6
	- 12 V	7
	Level tracking	8
	⏚	9
	+ 10 dB pad control signal	10
	Amplifier centring (R2)	11
	Rectifying bridge current	12
	Sampling control	13
	D2	14
	A1	15
	D1	16
	Regulation 2 +	17
	Filter tracking	18
	Regulation 2 -	19
	Doubler control	20

REMOVING THE OUTPUT MODULE
(to obtain access to amplifier board or for replacement)

a) Remove the rear and righthand side panels (meterside)
b) Unscrew the knurled ring to breaker
c) Unscrew and remove the rigid coaxial link between the VHF and output modules
d) Remove the fixing screws from the righthand side-cheek. Carefully withdraw the output module through the rear of the instrument, to avoid damaging the bypasses mounted on the bottom of the VHF module
If replacing the module insert the new unit and make all connections by carrying out the above procedure in reverse oder
For maintenance operations remove the cover to obtain access to the amplifier board. The VHF and output modules are connected by means of a coaxial extension cable

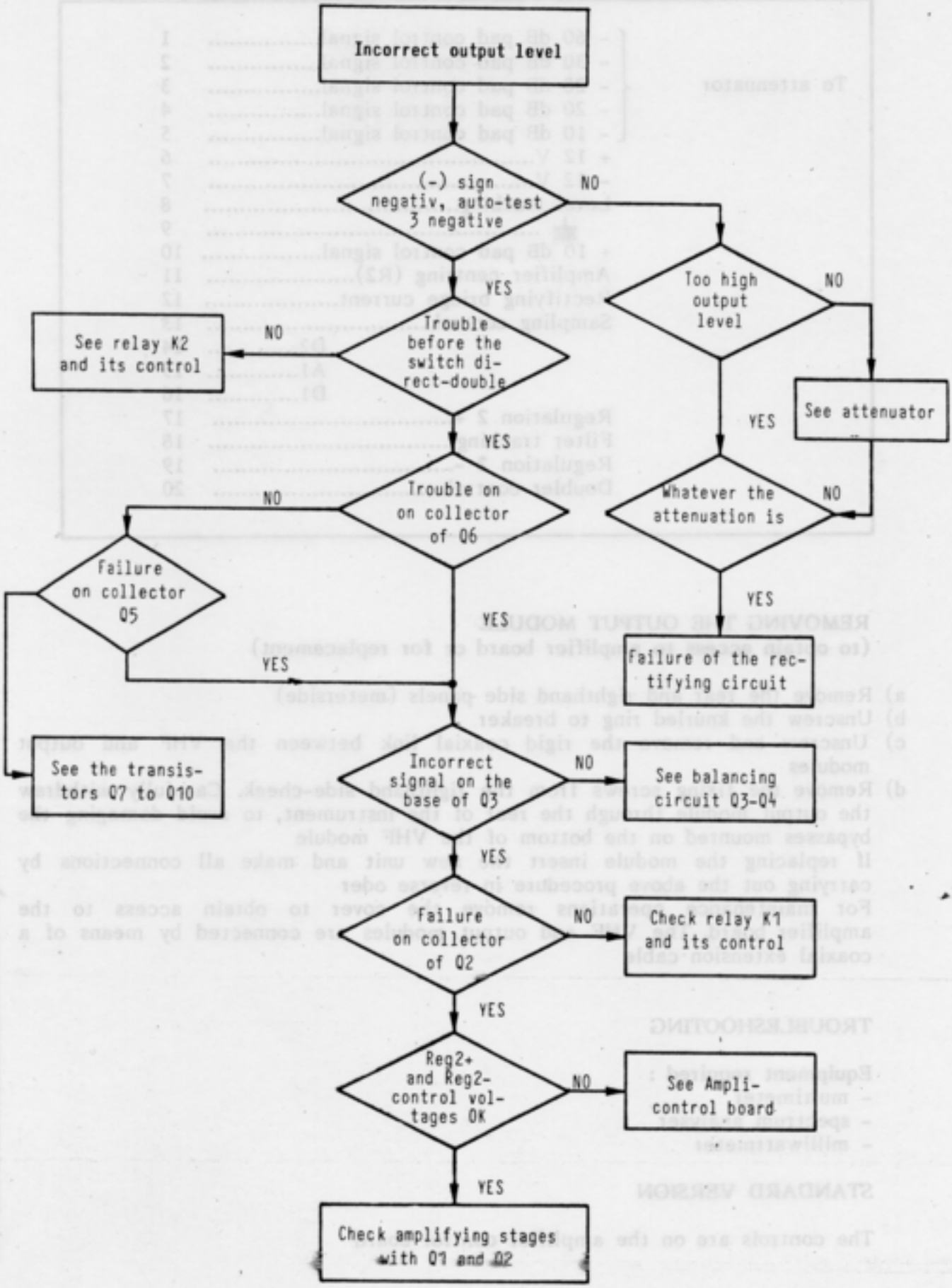
TROUBLESHOOTING

Equipment required :
- multimeter
- spectrum analyser
- milliwattmeter

STANDARD VERSION

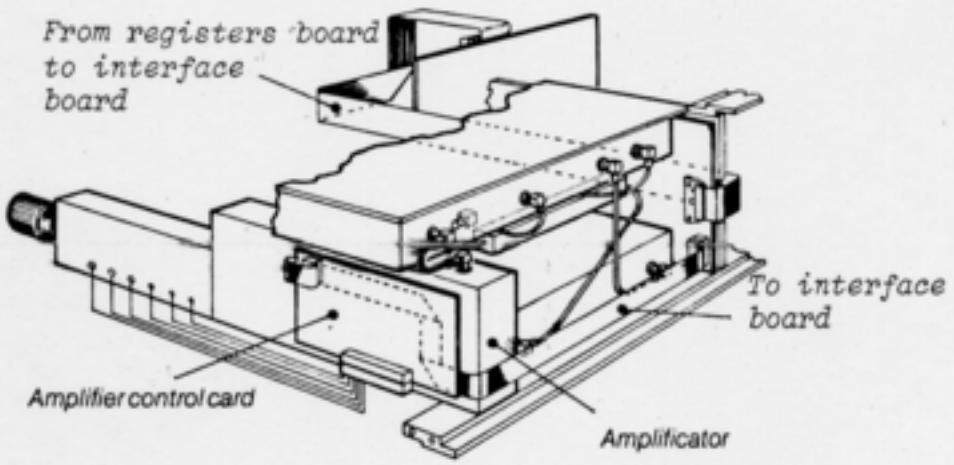
The controls are on the amplifier control board

TROUBLESHOOTING - Level failure



CONNECTOR PIN-OUT
CDE AMPLI/INTERFACE

- 12 V	1
- 12 V	2
+ 12 V	3
Tracking filter control, from VHF module.	4
Regulator 2 control, from analogue front panel	5
Detection to interface	6
Cell + 10 dB control from registers board.	7
⏚	8
- 60 dB cell control	9
- 30 dB cell control	10
- 20 dB cell control	11
- 20 dB cell control	12
- 10 dB cell control	13
Doubler validation (003 option)	14
+ 5 V	15
+ 18 V	16



AMPLIFIER AMPLI-ATTENUATOR CONTROL

ADJUST-CHECK

Required equipment :
-Subvis coaxial extender,
- Digital multimeter,
- RF milliwattmeter,
- 1.5 GHz. spectrum analyser,
- Network or amplitude analyser associated with a 1.5 GHz. wobulator.

1) **Check the resistance** between the emitters of each TP 3094 and - 12 V (9 ohms < R < 9.5 ohms). Same measurement on the emmiters of each TPV 596 and - 12 V (4.3 ohms < R < 4.7 ohms)
2) **Check the bias voltage** of the final stage with respect to - 12 V
   a) Emmiters of the TP 3094 : 0.9V < U < 1V)
   b) Emitters of the TPV 596 : 0.8V < U < 0.9V)
   Adjust these voltages if necessary in bridging either R42 or R43 by a resistor
3) **Amplifier centring**
   Adjust P1 so as to obtain the minimal H2 distortion whithin the range 0.3 to 650 MHz
4) **Regulation 2**
   Display 100 MHz, + 13 dBm on the range 10 dBm. Adjust P5 so that the voltage "U Reg 1" does not significantly vary in passing from + 13 to + 4 dBm, dB by dB
5) **For all adjustments**, refer to the chapter V : "Calibration"
6) **SWR measurement**
   This measurement is carried-out in the absence of the input signal. Connect the output of the attenuator to a directive coupler, connected itself to the wobulator. The output SWR, measured whithin the range 1 to 650 MHz must be equal or less than 2 with no attenuation, or equal or less than 1.5 with attenuation
   Whithin the range 650-1300 MHz the measured SWR must be in the first case equal or less than 2, and equal or less than 1.6 in the second case

ELECTRONIC BREAKER

The generator attenuator and amplifier are protected by an output relay controlled by an operational amplifier. The signal is input to a peak detector through a capacitive divider C4 - C5. The detected signal is applied to the input of amplifier SN1 which energises the relay.

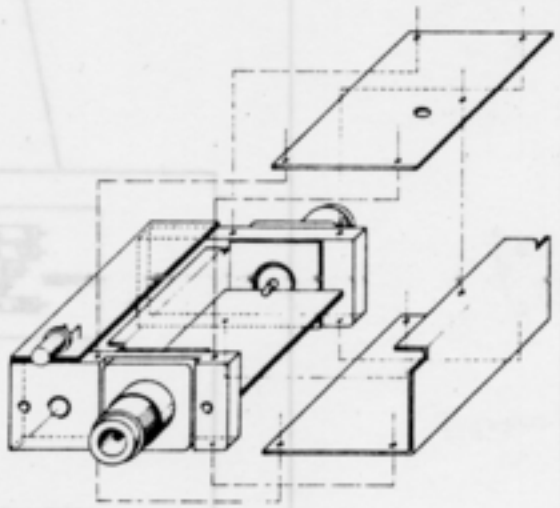
The option includes an instantaneous protection facility to enhance instrument security, especially during the interval required to open-circuit the output connection.

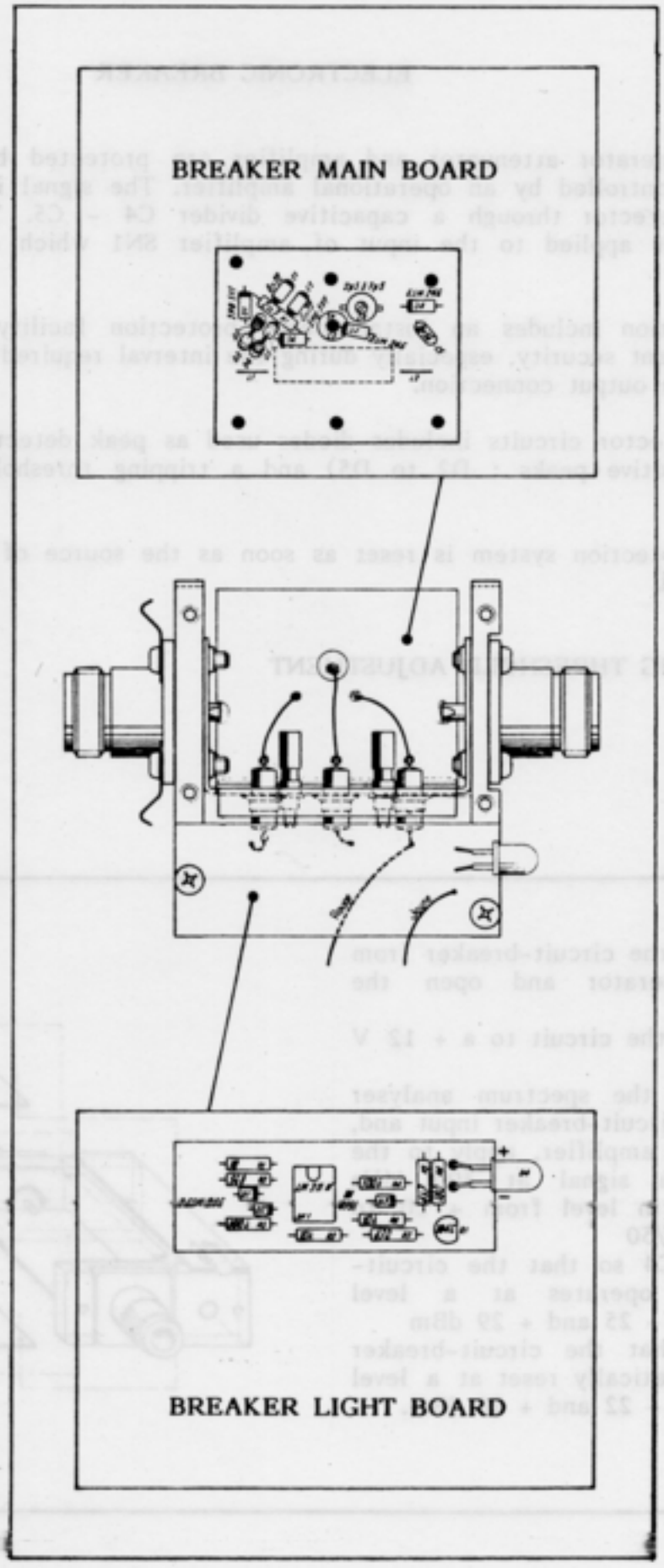
The detector circuits includes diodes used as peak detectors (negative and positive peaks : D2 to D5) and a tripping threshold dissipation circuit.

The protection system is reset as soon as the source of disruption is removed.

TRIPPING THRESHOLD ADJUSTMENT

a) Remove the circuit-breaker from the generator and open the casing
b) Connect the circuit to a + 12 V supply
c) Connect the spectrum analyser to the circuit-breaker input and, using an amplifier, apply to the output a signal at 300 MHz variable in level from + 20 to + 30dBm/50
d) Adjust C4 so that the circuit-breaker operates at a level between + 25 and + 29 dBm
e) Check that the circuit-breaker is automatically reset at a level between + 22 and + 26 dBm.




BREAKER MAIN BOARD
BREAKER LIGHT BOARD

OPTION 004

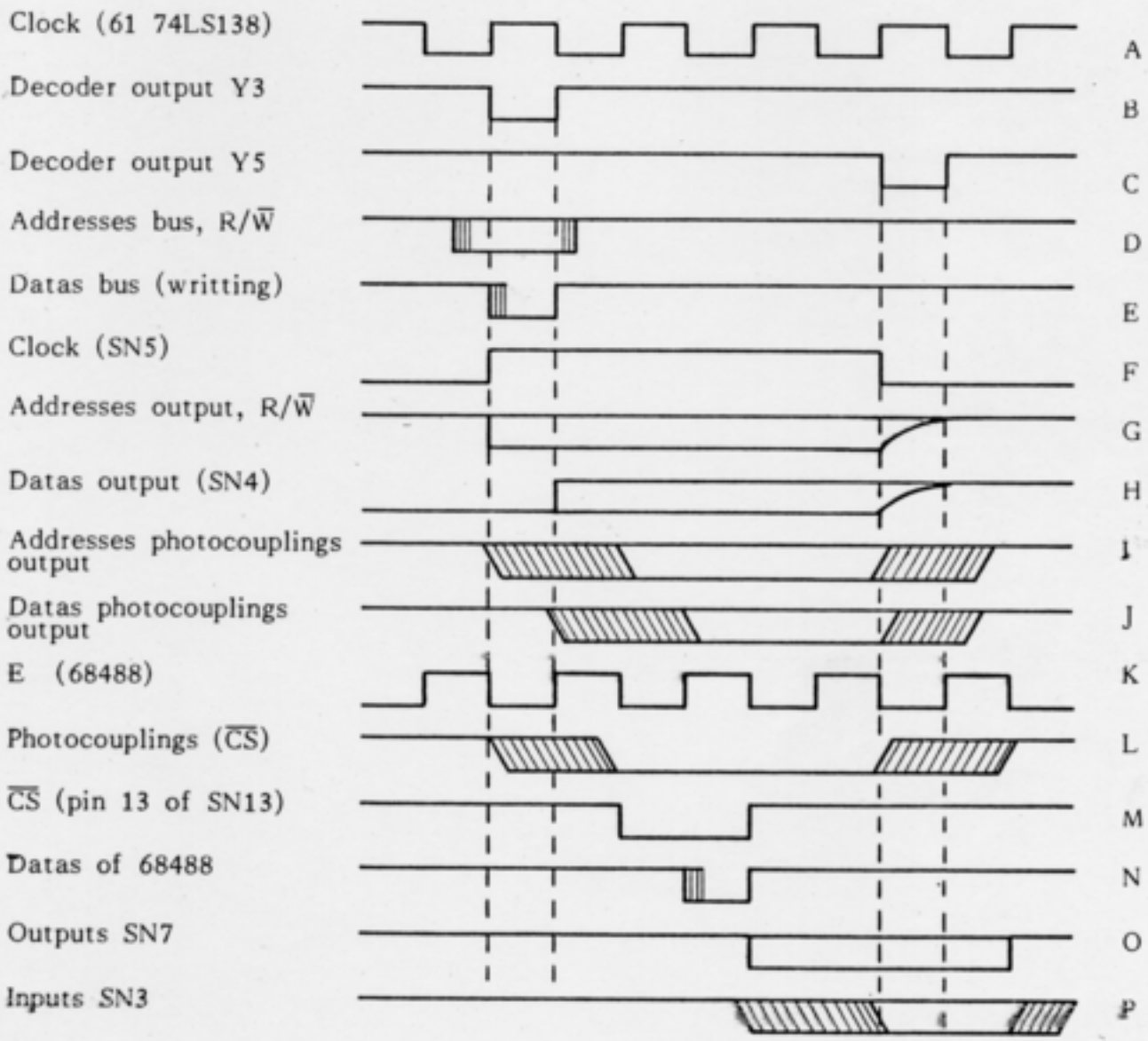
IEEE PROGRAMMING

This board insulates signals coming from IEEE Bus. The 1 MHz clock transits through the transforming T1 (with an inversion k). On the one of the 68488 registers writing, Y3 of decoder 74LS138 (B) passes over "0" validating so the addresses and the R/$\overline{W}$ on the SN5 (G) output. This informations convey through photocouplings, with a time about 1 s(I).

* Note that the datas(SN4) are differed of 0.5 s (H) by the step up of Y3(B). The information "0" pin 6 of SN28 valides the chip select of 68488 (L and M) realising the writing in the register. A reading (C) (who is not considered revalidates the SN6 sweep circuit and replaces the SN15 sweep circuit JK $\overline{Q}$ (pin 8) at "1".

For the reading, the addresses transmission at 68488 is the same that the previous writing : the first reading of the board is not considered by the CP1, it only fills the addresses at 68488 with the decoder Y3 (SN1) output. To read effectively the datas, a second reading by Y5 (SN1) is necessary and it is this one who is considered by the CPU.

CHRONOGRAM



PULSE MODULATION (OPTION 006)

The control pulses are simultaneously input to a threshold amplifier and a timer which respectively enable the modulator and level regulator.

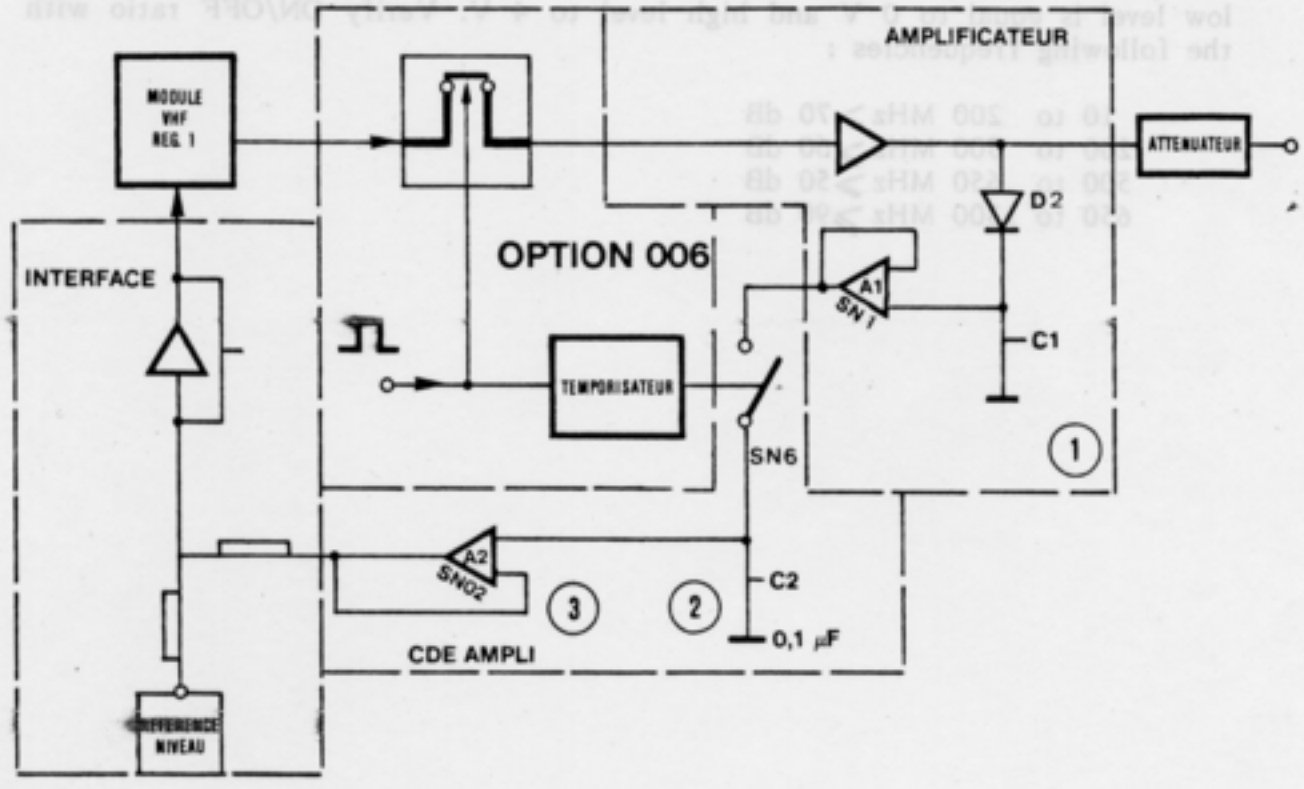
The threshold amplifier (Q6, Q7) is followed by a diode signal-shaping circuit D4, D5. The output pulses are transmitted to the modulator which chops the HF signal at the rate of the latter by means of a balanced amplifier of variable slope. The modulator is operated virtually from the start of the pulse (low threshold 0.35 V).

Level regulation is simultaneously provided by applying the pulse signal to the input of the + timer - which controls MOS switch SN6. Closing of this switch is retarded by 2 s so as to correspond to the complete charge of C1 (peak value of the signal).

When SN6 closes the charge on C1 is transferred into C2 (0.1 F) through SN1, an operational amplifier with high input impedance and low output impedance. This detected level is conformed, then routed across the going down impedance SN3 to the "INTERFACE" board, where it is compared with the impedance reference voltage.

Opening of the switch is also retarded relative to the falling edge of the pulse to improve the efficiency of the detector (time-delay due to R18, R19, C1 and Q6).

BLOCK DIAGRAM



ADJUSTMENTS

Preparation

* The access to circuit can only be possible after removing the output unit from the instrument.
* Remove the top and bottom, righthand side and rear panels.
* Disconnect all coaxial connections from the unit and remove following the procedure described for the amplifier.
* Remove the cover and reconnect all connections by means of extenders.

PULSE

MODULE REPAIRED

Equipment required
- Milliwattmeter,
- spectrum analyser.

1) Adjustment and level control
Short-circuit PT1 of the "Analog Front Panel" board. See chapter "CALIBRATION", paragraph 7

2) ON/OFF ratio control
a) Close the option
b) Connect analyser to attenuator output
c) Inject on the BNC socket, a modulating signal very low frequency, which low level is equal to 0 V and high level to 4 V. Verify ON/OFF ratio with the following frequencies :

10 to 200 MHz $\geq$ 70 dB
200 to 500 MHz $\geq$ 60 dB
500 to 650 MHz $\geq$ 50 dB
650 to 1300 MHz $\geq$ 90 dB

MAIN POWER SUPPLY

The power supply bloc includes :

- The mains filter with the voltage selector, and protection fuse,
- The transformer,
- The fan,
- The rectifying and smoothing circuits,
- The protection board,
- The regulation board.

This latter supply the regulated voltages : + 12 V, Pilot + 18 V, + 12 V, + 5 V, - 12 V and a floating power supply for the IEEE programming (Option 004) : about 13 V idle.

All sources except that of the IEEE option are protected against the short circuits.

The "Presence Power" is intended for the microprocessor information of either a mains drop, or the reset in stand-by of the instrument. It can therefore store the existing working configuration. For that reason, this voltage is filtered with a very short time-constant so as to vanish before all other power sources.

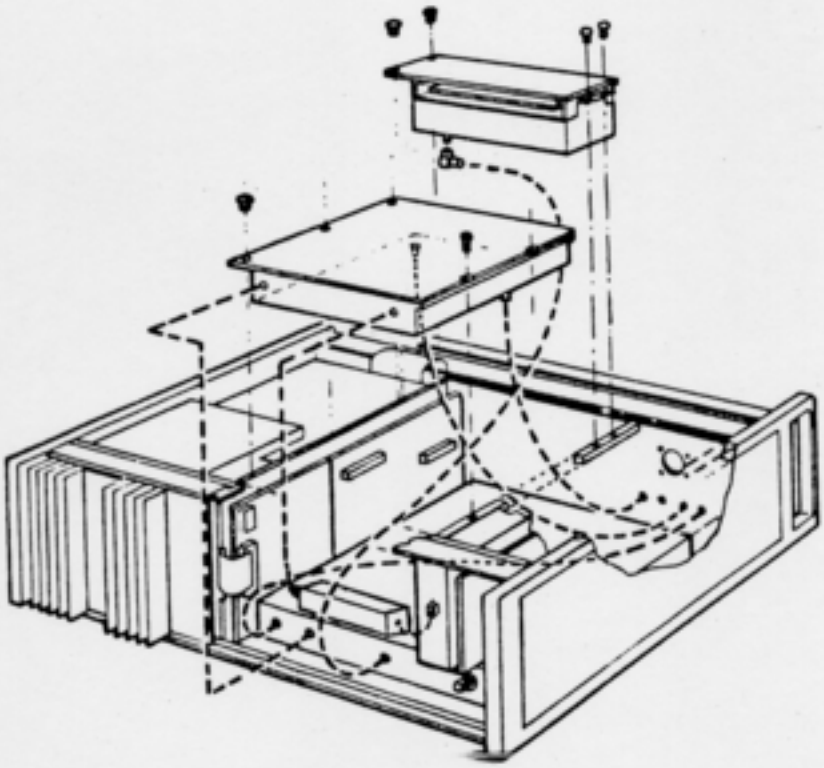
The "Protection" board limits the primary current on startup. This one is in fact very important due to the use of a toroidal transformer. This protection is achieved in introducing in series of two resistors of 22 ohms. After a few seconds these resistors are short-circuited by the relay. Closing of the latter is controlled by the "Presence Power" voltage and above all by the unregulated + 18 V.

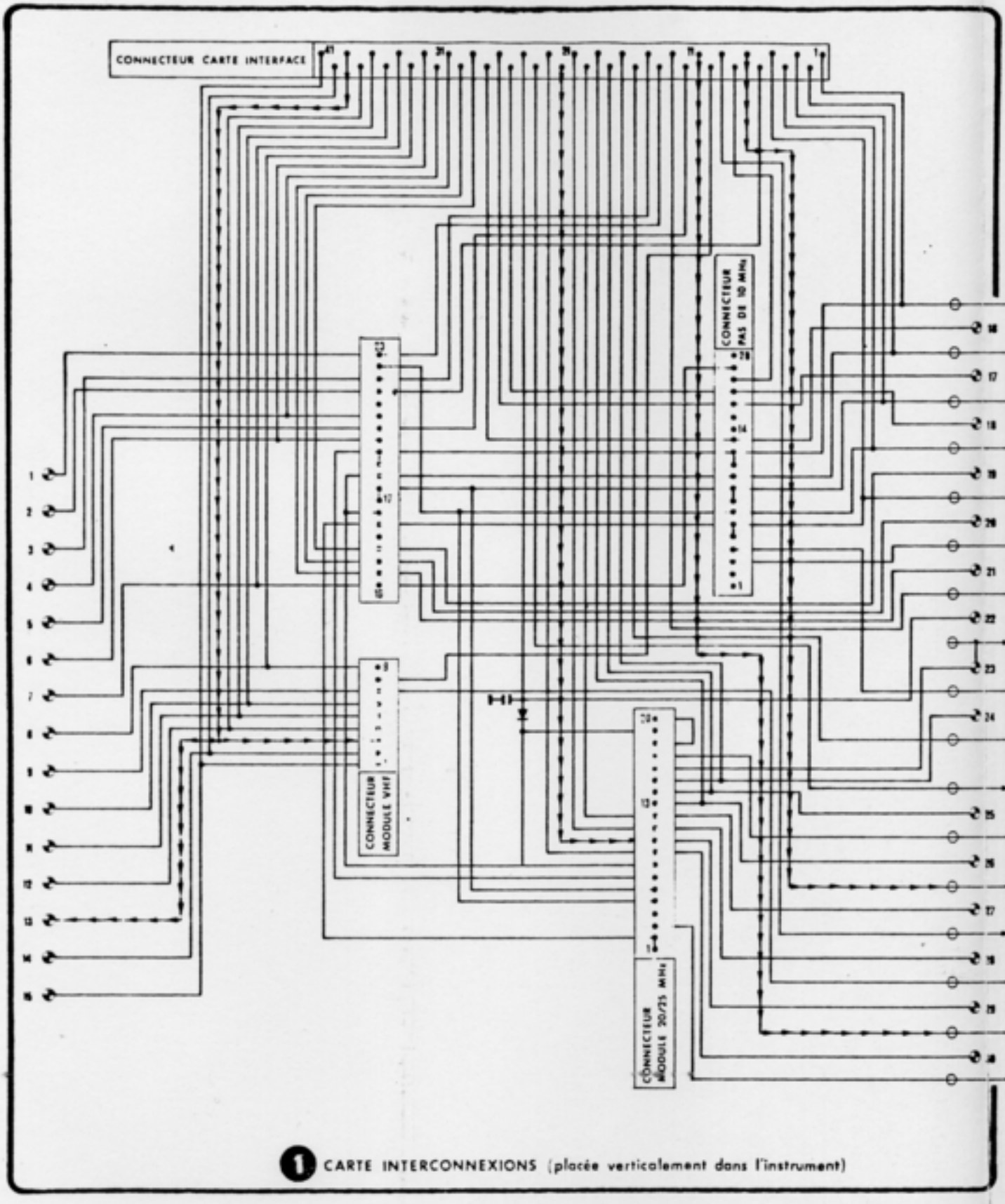
A thermal breaker in series with the "ON-OFF" switch stops the power supply in case of overheating of the instrument.

CONNECTOR PIN-OUT

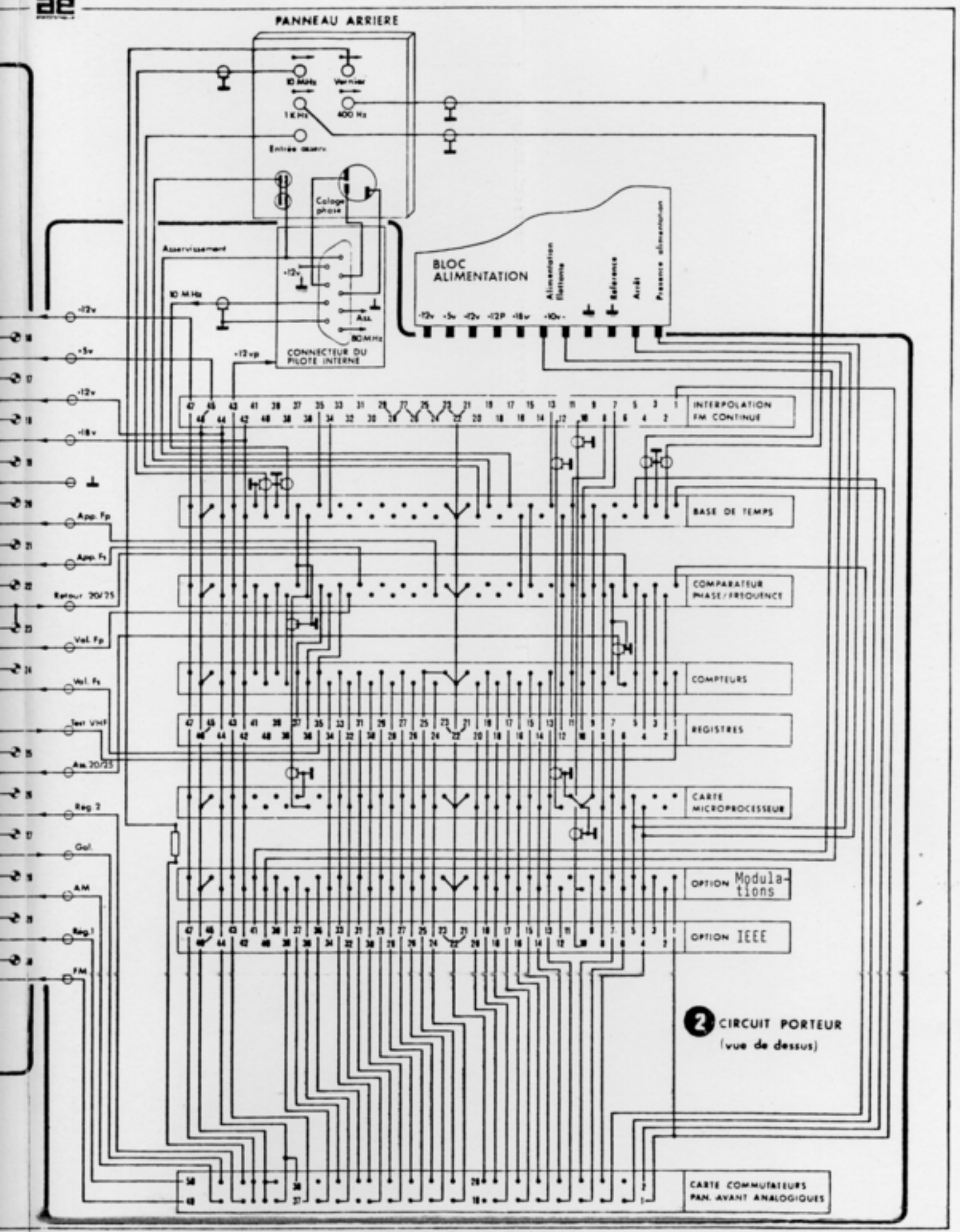
+ 18 V (non-regulated)	1
+ 18 V	2
+ 12 VP (pilot supply)	3
+ 5 V	4
+ 5 V	5
+ 5 V (non-regulated)	6
⏚	7
+ 12 V	8
+ 12 V	9
"Supply present" signal to CPU, protection and switch boards	10
"Supply absent" signal to option 004 and on/off switch	11
Supply present (non-regulated)	12
+ 12 V (non-regulated)	13
- 12 V	14
- 12 V	15
- 12 V (non-regulated)	16

INTERCONNECTIONS





1 CARTE INTERCONNEXIONS (placée verticalement dans l'instrument)

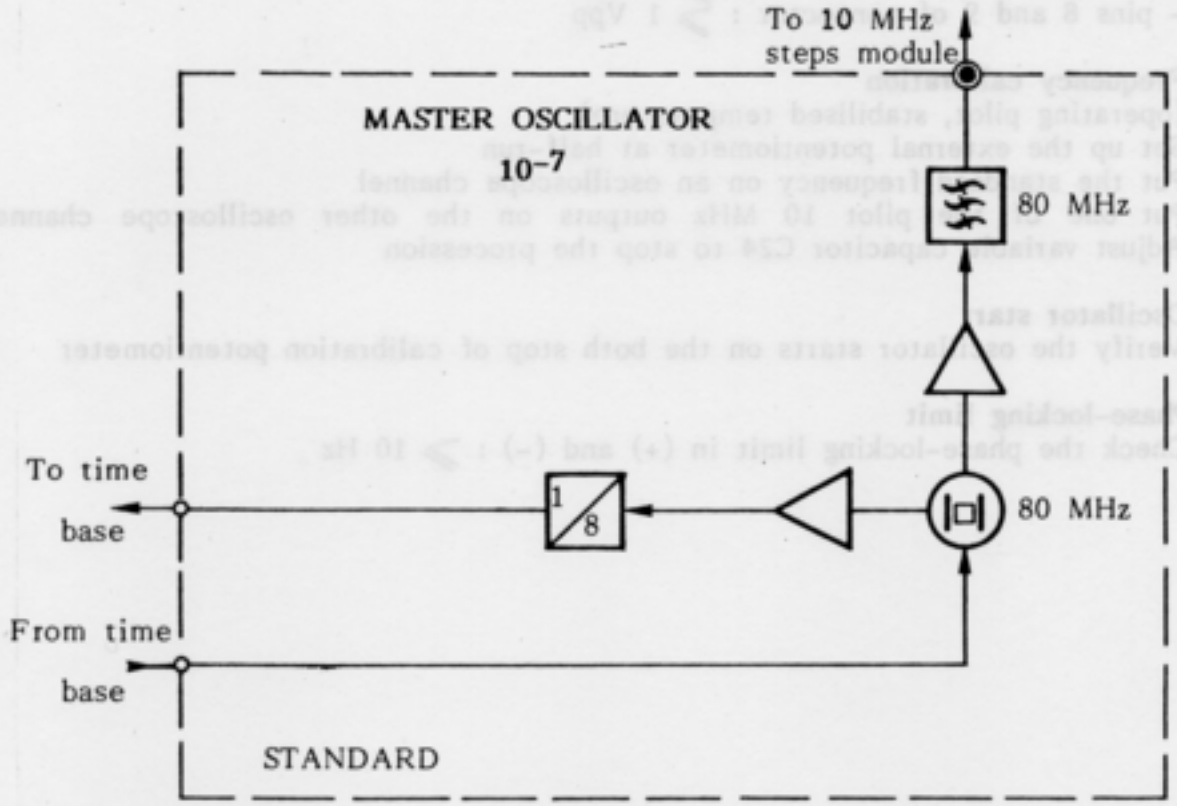


2 CIRCUIT PORTEUR
(vue de dessus)

7100 FACE AVANT

PILOTS

A) 80 MHz 10^{-7} standard pilot



ADJUSTMENT - CONTROL

Equipment required :
- Multimeter,
- 20 MHz oscilloscope,
- 1.5 GHz spectrum analyser,
- Frequency standard source (10 MHz or submultiple) which can vary of ± 20 Hz,
- Extender ribbon

1) Power supply control

a) Verify on pin 11 of SN2 : + 5 V ± 5%
b) Verify on pin 3 of connector : + 7 V ± 5%

2) Thermostat operating

After 5 minutes operating, verify the pilot consumption falls down of 400 mA max to less 250 mA

3) 80 MHz output filter

Connect spectrum analyser to 80 MHz output. Adjust T4 and T5 so as to obtain maximal level : + 2 dBm/50 ohms ± 2 dB
Check harmonic 2 : $\leq$ - 44 dB

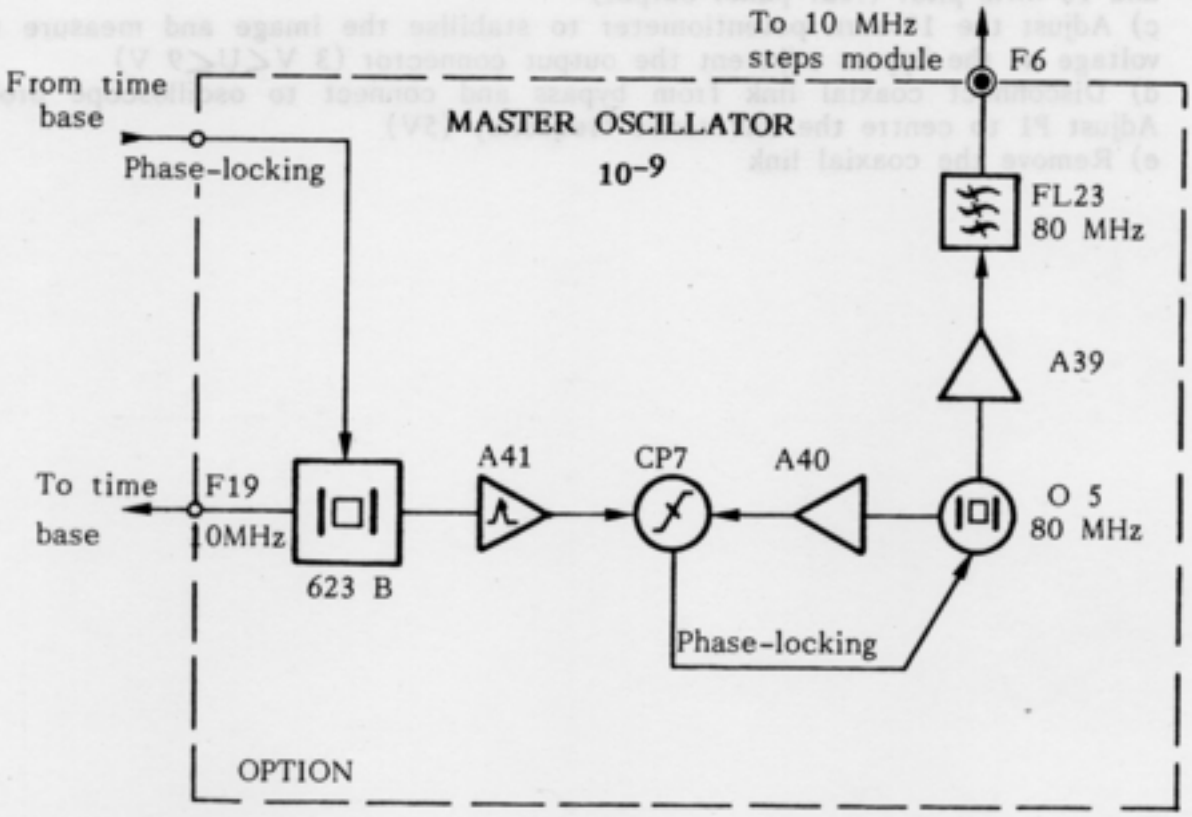
4) 10 MHz outputs
Verify level on outputs loaded by 100 ohms
- pins 4 and 5 of connector : $\geqslant$ 1 Vpp
- pins 8 and 9 of connector : $\leqslant$ 1 Vpp

5) Frequency calibration
(operating pilot, stabilised temperature)
Set up the external potentiometer at half-run
Put the standard frequency on an oscilloscope channel
Put one of the pilot 10 MHz outputs on the other oscilloscope channel
Adjust variable capacitor C24 to stop the procession

6) Oscillator start
Verify the oscillator starts on the both stop of calibration potentiometer

7) Phase-locking limit
Check the phase-locking limit in (+) and (-) : $\geqslant$ 10 Hz

B) 10^{-9} Pilot



ADJUSTMENT - CONTROL

Equipment required :
- Multimeter,
- Oscilloscope,
- Spectrum analyser.

1) 80 MHz filter adjustment

a) Solder 390 ohms resistor in parallel with T02 and set T01 to maximum
b) Desolder resistor and connect in parallel with T01. Set T02 to maximum
c) Remove resistor and connect spectrum analyser to module output. Verify that signal level is between + 2 and + 4 dBm

2) 80 MHz level

Verify that the 80 MHz level input to the "lock-on" circuit is - 5 dBm ± 1 (use 30 dB probe)

3) 10 MHz level

Verify that the 10 MHz level input to the "lock-on" circuit is + 3 dBm ± 1

4) Sum/difference frequency centring :

a) Lock generator onto external reference

b) Display Lissajou figure showing phase relationship of 10 MHz reference and 10 MHz pilot (rear panel output)

c) Adjust the 10-turn potentiometer to stabilise the image and measure the voltage at the bypass adjacent the output connector (3 V$\lesssim$U$\lesssim$9 V)

d) Disconnect coaxial link from bypass and connect to oscilloscope probe. Adjust P1 to centre the difference frequency (5V)

e) Remove the coaxial link

LOGIC BOARD

The logic board combines the four functions specific to the 7200A.

AUDIO FREQUENCY AMPLIFIER

The audio-frequency signal output from the interpolator is adjusted in amplitude over 10 dBm by means of AD7533 DAC SN8 connected to LM318 amplifier SN16. The output current of amplifier SN15 is increased by transistors Q1, Q2, Q11 and Q12 to drive the output attenuator on 50 by steps of 20 dBm. An analog cell of 10 dB is inserted into the link between the two amplifiers SN16 and SN15. Switching is performed by SN7 (4053 1/3).

CALIBRATION EPROM AND CMOS RAM

An address bus stored by 74C374 registers SN30 and SN31 supplies the addresses to the EPROM containing the correction coefficients, and to the save CMOS RAM memories. The data bus is stored upon writing by 74C374 register SN29, and amplified during reading by 74LS244 buffer SN28. A circuit enabling programming of the EPROM is made up of three 74LS26 NAND gates SN32, and by Q9 and Q10. The CMOS RAM is rescued by a 3.6 V Nicad accumulator when no external power is supplied to the equipment. When external power is supplied, transistor Q6 ensures supply of power to the RAM's, and charges the accumulator.

CALIBRATOR PEAK-TO-PEAK DETECTOR AND REMOTE CONTROL

A peak-to-peak amplitude detector ensures correct amplitude for the external modulating signal. This circuit drives two indicator lights located on the front panel of the equipment in the Modulations module, enabling adjustment of the signal applied to the external modulation inputs ; the circuit also warns the instrument microprocessor if the input signal amplitude is not calibrated in external modulation. The choice of AM or FM external modulation input is made by 4053 1/3 switch SN7. A first LF356 follower amplifier SN17 drives LM311 positive-peak and negative-peak double detector SN23 and SN24. The peak voltages detected are added by means of TL072 1/2 SN22, which drives TL072 1/2 inverser for amplification. Its output is sent to the front panel to control the two spade-head LED's indicating the direction necessary to calibrate the modulating signal, and to pins 12 and 13 of 74LS132 1/4 NAND gate SN14 to generate an interruption request to the microprocessor.

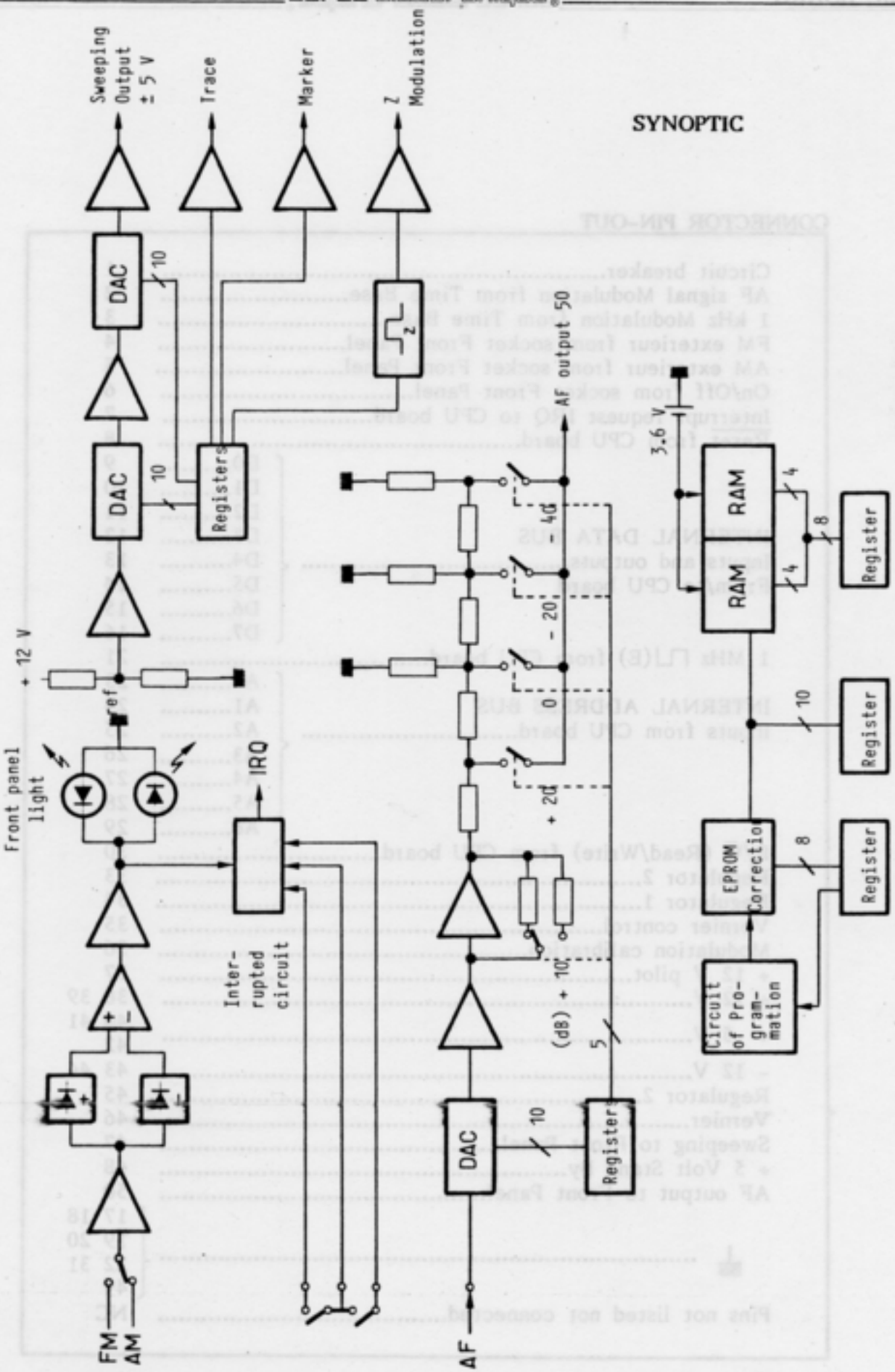
Sweeping remote control

The external pedal controls are limited in amplitude to + 5 V by D9 and D19, and at ground by D10 and D11. Two 4.7 µF capacitors, C36 and C37, filter the link with the pedal. These signals are applied to pins 9 and 10 of 74LS132 SN14 which triggers 4528 1/2 monostable SN13, causing an interruption request made by 4027 1/2 SN12.

SWEEPING

The Sweep module supplies, under microprocessor control, a gradient analog voltage available on the equipment front panel. Amplitude of the digital gradient is ± 5 V. An adjustable voltage reference made up by 1458 1/2 SN13 drives AD7533 DAC SN11. This DAC delivers a voltage which is incremented at each step ; the amplitude of the voltage range depends directly upon the number of sweeping steps. It is associated with 1458 1/2 amplifier SN19, which drives a second AD7533 DAC SN10, which in turn yields an inverse multiplying factor for the number of steps so as to always have constant gradient peak-to-peak amplitude of ± 5 V. This DAC is associated to 1458 1/2 amplifier SN18, which drives 1458 1/2 output amplifier SN18.

SYNOPTIC


Sweeping Output ± 5 V
Trace
Marker
Z Modulation
DAC
10
DAC
10
Registers
Z
AF output 50
3.6 V
RAM
RAM
4
4
8
Register
+ 12 V
ref
- 40
- 20
0
+ 20
10
Register
Front panel light
IRQ
EPROM Correctio
8
Register
Inter-rupted circuit
(dB) + 10
5
Circuit of Pro-gram-mation
DAC
10
Register
FM
AM
AF

CONNECTOR PIN-OUT

Circuit breaker		1
AF signal Modulation from Time Base		2
1 kHz Modulation from Time Base		3
FM exterieur from socket Front Panel		4
AM exterieur from socket Front Panel		5
On/Off from socket Front Panel		6
Interrupt request IRQ to CPU board		7
Reset from CPU board		8
INTERNAL DATA BUS Inputs and outputs From/to CPU board	D0	9
	D1	10
	D2	11
	D3	12
	D4	13
	D5	14
	D6	15
	D7	16
1 MHz ⊓⊔(E) from CPU board		21
INTERNAL ADDRESS BUS Inputs from CPU board	A0	23
	A1	24
	A2	25
	A3	26
	A4	27
	A5	28
	A6	29
R/$\overline{W}$ (Read/Write) from CPU board		30
Regulator 2		33
Regulator 1		34
Vernier control		35
Modulation calibration		36
+ 12 V pilot		37
+ 12 V		38 39
+ 5 V		40 41 42
- 12 V		43 44
Regulator 2		45
Vernier		46
Sweeping to Front Panel		47
+ 5 Volt Stand By		48
AF output to Front Panel		50
⏚		17 18 19 20 22 31 49
Pins not listed not connected		NC

BOARD ADJUSTMENT

Equipment required

- 1 multimeter,
- 1 RMS milliwattmeter,
- 1 oscilloscope 75 MHz (with rear socket Z axis input),
- 1 7200 mainframe (charged battery) with Modulations board adjusted.

Nota : Take off the EPROM 2716 SN33.

1) Check of memory voltage

a) The power supply being disconnected, connect the multimeter on R59 (330 Ω), side transmitter of Q6, read 3.6 V ± 1%.
b) Check the consummation of the RAM with measuring the voltage at terminals of R59 < 33 mV, i. e. < 100 μA.
c) Connect the power supply and measure on R59, side transmitter of Q6, about 5 V.

2) Check of AF amplifier

a) Validate the AF generator at 1 kHz, output level + 20 dBm.
b) Connect the milliwattmeter charged on 50Ω and adjust P1 so as to obtain 2.24 V RMS.
c) Display + 10 dBm and adjust P2 so as to obtain 0.708 V RMS.
d) With displaying the followed levels, check to obtain :

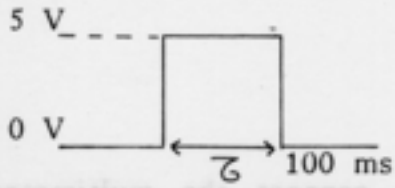
+ 5 dBm	398	mV RMS ± 5%
0 dBm	224	mV RMS ± 5%
- 10 dBm	70.8	mV RMS ± 10%
- 20 dBm	22.4	mV RMS ± 10%
- 30 dBm	7.08	mV RMS ± 10%
- 40 dBm	2.24	mV RMS ± 10%
- 50 dBm	0.708	mV RMS ± 10%
- 60 dBm	0.224	mV RMS ± 10%

3) Check of Detector - Calibrator

a) Validate the AM or FM socket in DC ext.
b) Inject it with the AF generator, a 1 kHz signal on the socket previously selected.
c) Connect the multimeter in AC on PT1, adjust the AF generator so as to read 1 V RMS. Check the level in PT2.
d) Connect the multimeter in DC and check PT4 + 1.41 V and PT3 - 1.41 V.
e) Connect the multimeter in D6 on PT6 and adjust P4 so as to obtain 0 V (balancing of two lights of the front panel).
f) Change the input of modulation and commutate the display on the selected input by FM (kHz) or AM% and check the balancing in PT6.

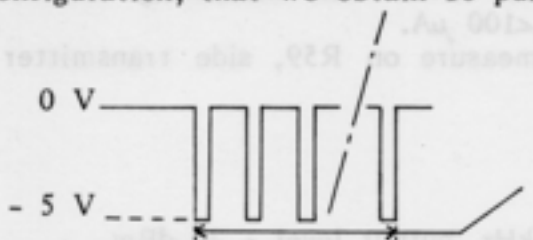
4) Check of sweeping

a) Validate the sweep function (ex : choose Start 10 MHz, Stop 100 MHz, relaxed Mode /WWW , 100 steps and 2 ms by step). Adjust P5 to centre the output voltage, sweeping about 0 V.
b) Check of sweeping remains centered with varying the step number.
c) Adjust P3 so as to obtain 5 V on the pin 7 of SN19.
d) Check with the oscilloscope on the rear socket repered by ⎍⎍ with 10 ms by step and 10 steps, that the output is :

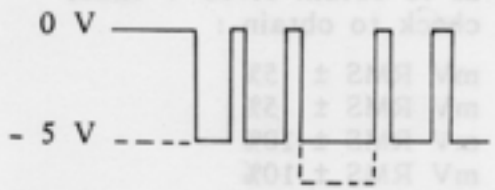


τ = temps par pas
X = nombre de pas

e) Check with the oscilloscope on the rear socket repered by ⎍ⵗ in the same configuration, that we obtain 10 pulses.



f) Display a frequency of Start 100 MHz, Stop 600 MHz, step number 5, speed 2 ms by step, a marker at 300 MHz, so as to obtain :



The marker level is depending on the potentiometer position between the two sockets ⎍ⵗ and ⵗ.

g) Check with the oscilloscope on the rear socket repered by ⵗ , the appearance of a positive pulse corresponding to each marker : exemple of the previous case.